RM551E-GL

Hardware Design

5G Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.

Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.

Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.

Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.

The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.

In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2023-12-12	Archibald JIANG/ Jerax KONG/ Devin WANG/ Jumping HE	Creation of the document
0.1	2024-01-09	Archibald JIANG/ Jerax KONG/ Devin WANG/ Jumping HE	Draft

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1 Introduction

1.1. Introduction

The document introduces RM551E-GL module and describes its air interface and hardware interfaces which are connected to your applications.

This document helps you quickly understand the interface specifications, RF characteristics, electrical and mechanical details, as well as other related information of the module. To facilitate its application in different fields, reference design is also provided for reference. Associated with application notes and user guides, you can use the module to design and set up mobile applications easily. You can also see ***document [1]*** to understand the module hardware architecture.

1.2. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, argument, and so on, it indicates that the function, feature, interface, pin, AT command, argument, and so on, is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.

2 Product Overview

2.1. Frequency Bands and Functions

RM551E-GL is a 5G NR/LTE-FDD/LTE-TDD/UMTS/HSPA+ wireless communication module with receive diversity. It supports embedded operating systems such as Windows, Linux and Android, and also provides GNSS (optional) and voice functions to meet specific application demands.

RM551E-GL is an industrial-grade module for industrial and commercial applications only.

Table 2: Basic Information

Category	
Package	Standard M.2 Key-B
Dimensions	30.0 mm × 52.0 mm × 2.3 mm
Weight	Approx. 9.6 g

Table 3: RM551E-GL Frequency Bands & MIMO & GNSS Systems

Mode	Frequency Bands
5G NR SA	n1/n2/n3/n5/n7/n8/n12/n13/n14/n18/n20/n25/n26/n28/n29/n30/n38/n40/n41/n48/n66/n70/n71/n75/n76/n77/n78/n79/n257/n258/n260/n261 **DL 4 × 4 MIMO**: n1/n2/n3/n7/n25/n30/n38/n40/n41/n48/n66/n70/n77/n78/n79 **UL 2 × 2 MIMO**: n38/n41/n48/n77/n78/n79
5G NR NSA	n1/n2/n3/n5/n7/n8/n12/n13/n14/n18/n20/n25/n26/n28/n29/n30/n38/n40/n41/n48/n66/n70/n71/n75/n76/n77/n78/n79/n257/n258/n260/n261 **DL 4 × 4 MIMO**: n1/n2/n3/n7/n25/n30/n38/n40/n41/n48/n66/n70/n77/n78/n79
LTE	FDD: B1/B2/B3/B4/B5/B7/B8/B12/B13/B14/B17/B18/B19/B20/B25/B26/B28/B29/B30/B32/B66/B71 TDD: B34/B38/B39/B40/B41/B42/B43/B46(LAA)/B48 **DL 4 × 4 MIMO**: B1/B2/B3/B4/B7/B25/B30/B38/B40/B41/B42/B43/B48/B66

WCDMA	B1/B2/B4/B5/B8/B19
GNSS	GPS/GLONASS/BDS/Galileo/QZSS

2.2. Key Features

Table 4: Key Features of RM551E-GL

Feature	Details
Function Interface	● PCI Express M.2 Interface ● Compliant with *PCI Express M.2 Specification Revision 4.0*
Power Supply	● 3.135–4.4 V ● Typ.: 3.7 V
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
USB Interface	● Compliant with USB 3.1 Gen 2 and USB 2.0 specifications ● Maximum transmission rates: – USB 3.1 Gen 2: 10 Gbps – USB 2.0: 480 Mbps ● Use: AT command communication, data transmission, firmware upgrade, software debugging, GNSS NMEA sentence output and voice over USB* ● Supported USB serial drivers: – Windows 8/8.1/10/11 – Linux 2.6–6.5 – Android 4.x–13.x
(U)SIM Interface	● Compliant with *ISO/IEC 7816-3*, ETSI and IMT-2000 ● Supported (U)SIM card: Class B (3.0 V) and Class C (1.8 V) ● Dual SIM Single Standby
eSIM	Optional eSIM function
PCIe Interface	● PCIe × 1 lane, supporting up to 16 Gbps ● Compliant with PCIe Gen 4 ● Use: AT command communication, data transmission, firmware upgrade, software debugging, GNSS NMEA sentence output
Antenna Interfaces	ANT0, ANT1, ANT2, and ANT3

Transmitting Power [1]	● 5G NR bands: Class 3 (23 dBm ±2 dB) ● 5G NR HPUE [2] bands (n38/n40/n41/n77/n78/n79): Class 2 (26 dBm +2/-3 dB) ● 5G NR HPUE [2] bands (n41/n77/n78/n79): Class 1.5 (29 dBm +1/-2 dB) ● 5G NR mmWave bands (n257/n258/n260/n261): Class 3 ● LTE bands: Class 3 (23 dBm ±2 dB) ● LTE HPUE [2] bands (B38/B41/B42/B43): Class 2 (26 dBm ±2 dB) ● WCDMA bands: Class 3 (23 dBm ±2 dB)
5G NR	- Compliant with 3GPP Rel-16 specification - Modulations: - Sub-6 GHz UL: π/2-BPSK, QPSK, 16QAM, 64QAM and 256QAM - Sub-6 GHz DL: QPSK, 16QAM, 64QAM and 256QAM - mmWave Uplink: π/2-BPSK, QPSK, 16QAM, 64QAM - mmWave Downlink: QPSK, 16QAM, 64QAM and 256QAM - SCS: 15 kHz (FDD) , 30 kHz (TDD) - SCS: 120kHz (mmWave) - DL 4 × 4 MIMO and UL 2 × 2 MIMO **NSA and SA:** - Option 3x, 3a, 3 and Option 2 - Max. data rates [3]: - NSA Sub-6 GHz: 5.47 Gbps (DL), 730 Mbps (UL) - SA Sub-6 GHz: 7.01 Gbps (DL), 1.25 Gbps (UL) - NSA mmWave: 9.41 Gbps (DL)/3.66 Gbps (UL) - SA mmWave: 8.61Gbps (DL) / 3.54Gbps (UL) - SRS: - NSA: 1T4R (n38/n40/n41/n48/n77/n78/n79) - SA: 2T4R (n38/n41/n48/n77/n78/n79)
LTE	● Compliant with 3GPP Rel-16 specification ● Max. LTE category: Cat 20 (DL), Cat 18 (UL) ● Supported RF bandwidth: 1.4/3/5/10/15/20 MHz ● Modulations: - UL: QPSK, 16QAM and 64QAM and 256QAM - DL: QPSK, 16QAM and 64QAM and 256QAM ● DL 4 × 4 MIMO ● Max. data rates [3]: 2.0 Gbps (DL), 211 Mbps (UL)
UMTS Features	● Complaint with 3GPP Rel-9 specification ● DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA ● Modulations: QPSK, 16QAM and 64QAM ● Max. data rates [3]: - DC-HSDPA: 42 Mbps (DL)

[1] PC2 and PC1.5 are not available in Japan due to the local regulations.
[2] HPUE is only for single carrier.
[3] The maximum rates are theoretical and the actual values refer to the network configuration.

	- HSUPA: 5.76 Mbps (UL) - WCDMA: 384 kbps (DL), 384 kbps (UL)
Rx-diversity	5G NR/LTE/WCDMA
GNSS Features	● GPS/GLONASS/BDS/Galileo/QZSS ● Dual-band GNSS: L1 and L5 ● Compliant with NMEA 0183 protocol ● Data Update Rate: 1 Hz by default
AT Commands	● Compliant with *3GPP TS 27.007* and *3GPP TS 27.005* ● Quectel enhanced AT commands
Internet Protocol	● NITZ, PING and QMI protocols ● PAP and CHAP for PPP connections
Firmware Upgrade	● USB 2.0 & USB 3.1 interface ● PCIe interface ● FOTA*
Temperature Range	● Normal operating temperature: -30 °C to +75 °C [4] ● Extended operating temperature: -40 °C to +85 °C [5] ● Storage temperature: -40 °C to +90°C
RoHS	All hardware components are fully compliant with EU RoHS directive

2.3. Functional Diagram

The following figure shows a block diagram of RM551E-GL

- Power management
- Baseband
- LPDDR4X SDRAM + NAND Flash
- Radio frequency
- M.2 Key-B interface

[4] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heat sinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

[5] To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heat sinks, heat pipes, vapor chambers. Within this range, the module retains the ability to establish and maintain functions such as voice*, SMS, data transmission and emergency call*, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as Pout, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

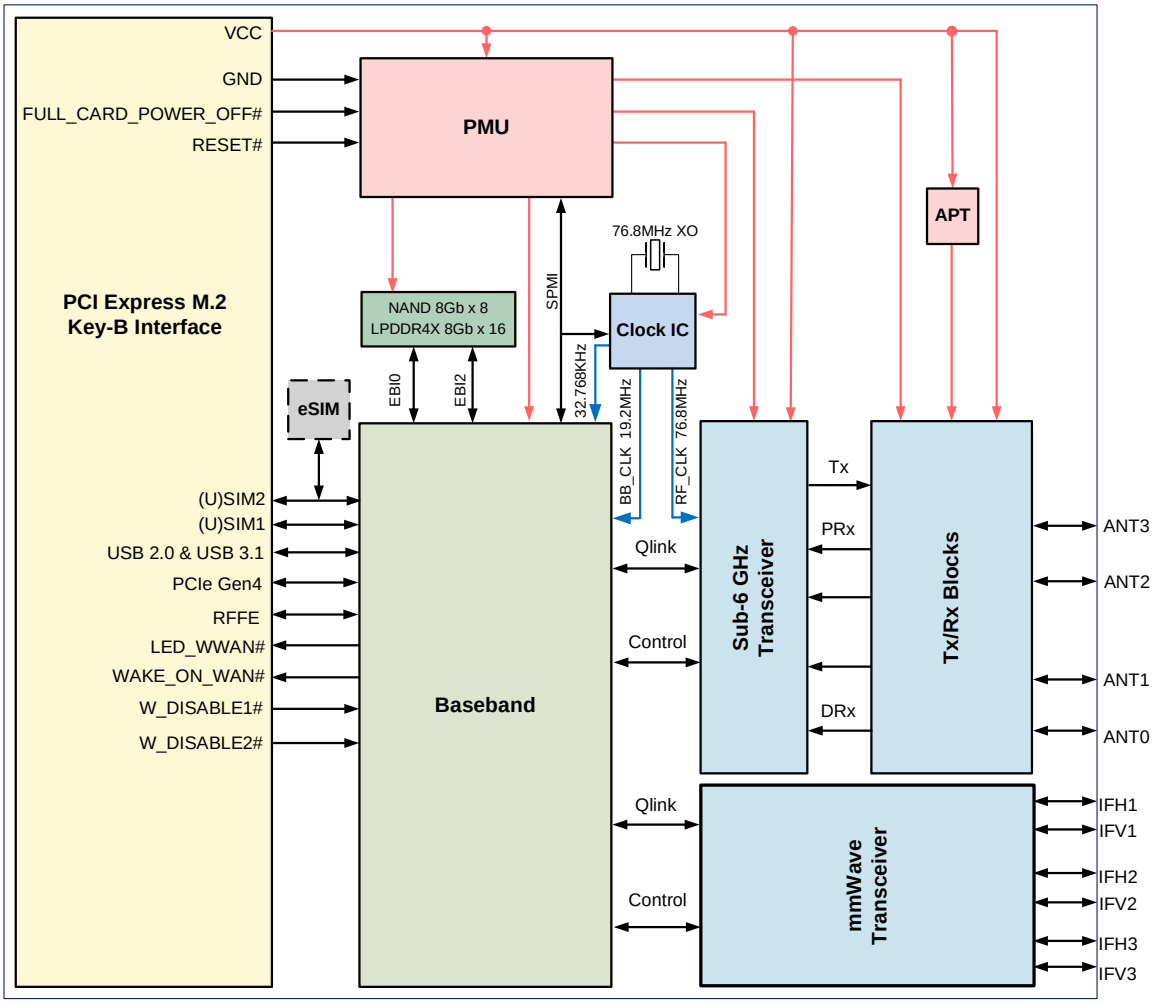
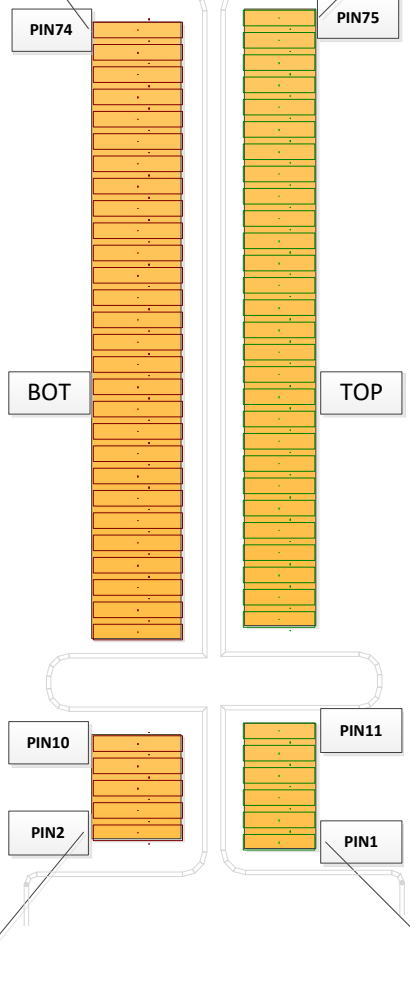


Figure 1: Functional Diagram

2.4. Pin Assignment

No.	Pin Name
74	VCC
72	VCC
70	VCC
68	RESERVED
66	USIM1_DET
64	COEX_TXD
62	COEX_RXD
60	N79_TX_EN
58	RFFE_DATA
56	RFFE_CLK
54	PEWAKE#
52	CLKREQ#
50	PERST#
48	USIM2_VDD
46	USIM2_RST
44	USIM2_CLK
42	USIM2_DATA
40	USIM2_DET
38	WLAN_TX_EN
36	USIM1_VDD
34	USIM1_DATA
32	USIM1_CLK
30	USIM1_RST
28	RESERVED
26	W_DISABLE2#
24	VDDIO_1V8
22	RESERVED
20	RESERVED
	Notch
	Notch
	Notch
	Notch
10	LED_WWAN#
8	W_DISABLE1#
6	FULL_CARD_POWER_OFF#
4	VCC
2	VCC



Pin Name	No.
CONFIG_2	75
VIO_CFG	73
GND	71
CONFIG_1	69
RESET#	67
QTM_VDD_1V9	65
QTM2_PON	63
QTM1_PON	61
QTM0_PON	59
GND	57
PCIE_REFCLK_P	55
PCIE_REFCLK_M	53
GND	51
PCIE_RX_P	49
PCIE_RX_M	47
GND	45
PCIE_TX_P	43
PCIE_TX_M	41
GND	39
USB_SS_RX_P	37
USB_SS_RX_M	35
GND	33
USB_SS_TX_P	31
USB_SS_TX_M	29
GND	27
DPR	25
WAKE_ON_WAN#	23
CONFIG_0	21
Notch	
Notch	
Notch	
Notch	
GND	11
USB_DM	9
USB_DP	7
GND	5
GND	3
CONFIG_3	1

Figure 2: Pin Assignment

NOTE

Keep all RESERVED and unused pins unconnected.

2.5. Pin Description

Table 5: Parameter Definition

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 6: Pin Description

Pin No.	Pin Name	I/O	Description	DC Characteristic	Comment
1	CONFIG_3	DO	Not connected internally		
2	VCC	PI	Power supply for the module	Vmin = 3.135 V Vnom = 3.7 V Vmax = 4.4 V	
3	GND		Ground		
4	VCC	PI	Power supply for the module	Refer to pin 2	
5	GND		Ground		
6	FULL_CARD_ POWER_OFF#	DI	Turn on/off the module High level: Turn on	V_{IH}max = 3.6 V V_{IH}min = 1.19 V	Internally pulled down with a 100 kΩ resistor.

			Low level: Turn off	V_{IL}max = 0.2 V	
7	USB_DP	AIO	USB differential data (+)		A test point must be reserved.
8	W_DISABLE1#	DI	Airplane mode control Active LOW	1.8/3.3 V	
9	USB_DM	AIO	USB differential data (-)		A test point must be reserved.
10	LED_WWAN#	OD	RF status LED indicator Active LOW	VCC	
11	GND		Ground		
12	Notch		Notch		
13	Notch		Notch		
14	Notch		Notch		
15	Notch		Notch		
16	Notch		Notch		
17	Notch		Notch		
18	Notch		Notch		
19	Notch		Notch		
20	RESERVED				
21	CONFIG_0	DO	Not connected internally		
22	RESERVED				
23	WAKE_ON_WAN#	OD	Wake up the host Active LOW	1.8 V	
24	VDDIO_1V8	PO	Provide 1.8 V for external circuit	$I_O$max = 50 mA 1.8 V	
25	DPR	DI	Dynamic power reduction	1.8 V	
26	W_DISABLE2#*	DI	GNSS control Active LOW	1.8/3.3 V	
27	GND		Ground		
28	RESERVED				
29	USB_SS_TX_M	AO	USB 3.1 SuperSpeed		

			transmit (-)		
30	USIM1_RST	DO	(U)SIM1 card reset	USIM1_VDD	
31	USB_SS_TX_P	AO	USB 3.1 SuperSpeed transmit (+)		
32	USIM1_CLK	DO	(U)SIM1 card clock	USIM1_VDD	
33	GND		Ground		
34	USIM1_DATA	DIO	(U)SIM1 card data	USIM1_VDD	
35	USB_SS_RX_M	AI	USB 3.1 SuperSpeed receive (-)		
36	USIM1_VDD	PO	(U)SIM1 card power supply	**High-voltage** Vmax = 3.05 V Vnom = 2.85 V Vmin = 2.7 V **Low-voltage** Vmax = 1.95 V Vnom = 1.8 V Vmin = 1.65 V	
37	USB_SS_RX_P	AI	USB 3.1 SuperSpeed receive (+)		
38	WLAN_TX_EN*	DI	Notification from WLAN to SDR when WLAN transmitting	1.8 V	
39	GND		Ground		
40	USIM2_DET [6]	DI	(U)SIM2 card hot-plug detect	1.8 V	
41	PCIE_TX_M	AO	PCIe transmit (-)		Require differential impedance of 85 Ω.
42	USIM2_DATA	DIO	(U)SIM2 card data	USIM2_VDD	
43	PCIE_TX_P	AO	PCIe transmit (+)		Require differential impedance of 85 Ω.
44	USIM2_CLK	DO	(U)SIM2 card clock	USIM2_VDD	
45	GND		Ground		

[6] USIM1_DET and USIM2_DET are pulled LOW by default, and will be internally pulled up to 1.8 V by software configuration only when (U)SIM hot-plug is enabled by **AT+QSIMDET**. Please do not add a pull-up resistor to USIM_DET pin.

46	USIM2_RST	DO	(U)SIM2 card reset	USIM2_VDD	
47	PCIE_RX_M	AI	PCIe receive (-)		Require differential impedance of 85 Ω.
48	USIM2_VDD	PO	(U)SIM2 card power supply	**High-voltage** Vmax = 3.05 V Vnom = 2.85 V Vmin = 2.7 V **Low-voltage** Vmax = 1.95 V Vnom = 1.8 V Vmin = 1.65 V	
49	PCIE_RX_P	AI	PCIe receive (+)		Require differential impedance of 85 Ω.
50	PERST#	DI [7]	PCIe reset Active LOW	1.8/3.3 V	
51	GND		Ground		
52	CLKREQ#	OD [7]	PCIe clock request Active LOW	1.8/3.3 V	
53	PCIE_REFCLK_M	AIO	PCIe reference clock (-)		100 MHz. Require differential impedance of 85 Ω.
54	PEWAKE#	OD [7]	PCIe wake up Active LOW	1.8/3.3 V	
55	PCIE_REFCLK_P	AIO	PCIe reference clock (+)		100 MHz. Require differential impedance of 85 Ω.
56	RFFE_CLK* [8]	DO	Used for external MIPI IC control	1.8 V	
57	GND		Ground		
58	RFFE_DATA* [8]	DIO	Used for external MIPI IC control	1.8 V	
59	QTM0_PON	DO	mmWave antenna control 0	1.8 V	
60	N79_TX_EN*	DO	Notification from SDR to WLAN when n79 transmitting	1.8 V	

[7] PERST# behaves as DI in PCIe EP mode, and as OD in PCIe RC mode. CLKREQ# and PEWAKE# behave as OD in PCIe EP mode, and as DI in PCIe RC mode. PCIe EP mode is the default.
[8] If this function is required, please contact Quectel for more details.

61	QTM1_PON	DO	mmWave antenna control 1	1.8 V	
62	COEX_RXD* [9]	DI	5G/LTE and WLAN coexistence receive	1.8 V	
63	QTM2_PON	DO	mmWave antenna control 2	1.8 V	
64	COEX_TXD* [9]	DO	5G/LTE and WLAN coexistence transmit	1.8 V	
65	QTM_VDD_1V9	PO	mmWave antenna power supply	Vmin = 1.85 V Vnom = 1.904 V Vmax = 2.04 V	-
66	USIM1_DET [6]	DI	(U)SIM1 card hot-plug detect	1.8 V	
67	RESET#	DI	Reset the module Active LOW	1.8 V	Internally pulled up to 1.8 V. A test point is recommended to be reserved if unused.
68	RESERVED				
69	CONFIG_1	DO	Connected to GND internally		
70	VCC	PI	Power supply for the module	Refer to pin 2	
71	GND		Ground		
72	VCC	PI	Power supply for the module	Refer to pin 2	
73	VIO_CFG		Configuration of PCIe sideband signals [10] power domain NC: support 1.8/3.3 V; GND: support 3.3 V		The default state is NC (Not connected).
74	VCC	PI	Power supply for the module	Refer to pin 2	
75	CONFIG_2	DO	Not connected internally		

NOTE

[9] Please note that COEX_RXD and COEX_TXD cannot be used as general UART ports.
[10] PCIe sideband signals include PERST#, CLKREQ# and PEWAKE#.

Keep all RESERVED and unused pins unconnected.

2.6. EVB Kit

Quectel supplies an evaluation board (5G-mmWave-EVB) with accessories to control or test the module. For more details, see ***document [3]***.

3 Operating Characteristics

3.1. Operating Modes

The table below briefly summarizes the various operating modes of the module.

Table 7: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	The module remains registered on the network but has no data interaction with the network. In this mode, the software is active.
	Voice/Data	The module is connected to the network. In this mode, the power consumption is decided by network settings and data rates.
Minimum Functionality Mode	**AT+CFUN=0** can set the module to a minimum functionality mode without removing the power supply. In this mode, both RF function and (U)SIM card are invalid.	
Airplane Mode	**AT+CFUN=4** or driving W_DISABLE1# LOW can set the module to airplane mode. In this mode, RF function is disabled and all relevant AT commands are inaccessible.	
Sleep Mode	When **AT+QSCLK=1** command is executed and the host's USB enters suspended mode, the module will enter sleep mode. The module can still receive paging, SMS, voice call and TCP/UDP data from the network. In this mode, the power consumption of the module is reduced to an ultra-low level.	
Power Down Mode	PMU shuts down the power supply. In this mode, the software is inactive. However, the voltage supply (for VCC) remains connected.	

NOTE

For more details about the AT command, see ***document [4]***.

3.1.1. Sleep Mode

With DRX technology, power consumption of the module will be reduced to an ultra-low level. The figure below shows the relationship between the DRX run time and the power consumption in sleep mode. The

longer the DRX runs, the lower the power consumption is.

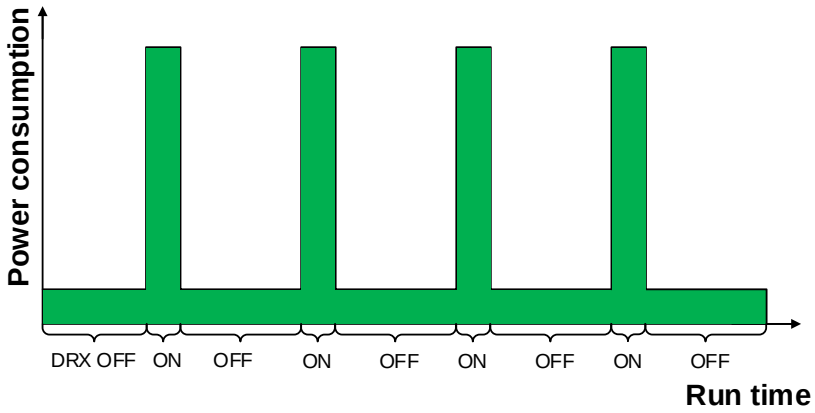


Figure 3: Module Power Consumption in Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

The following part of this section presents the power saving procedure and sleep mode of the module.

If the host supports USB suspend/resume and remote wakeup function, the following two conditions must be met to set the module to sleep mode.

- Execute **AT+QSCLK=1** command. For more details, see ***document [4]***.
- The module's USB interface enters suspended mode.

The following figure shows the connection between the module and the host.

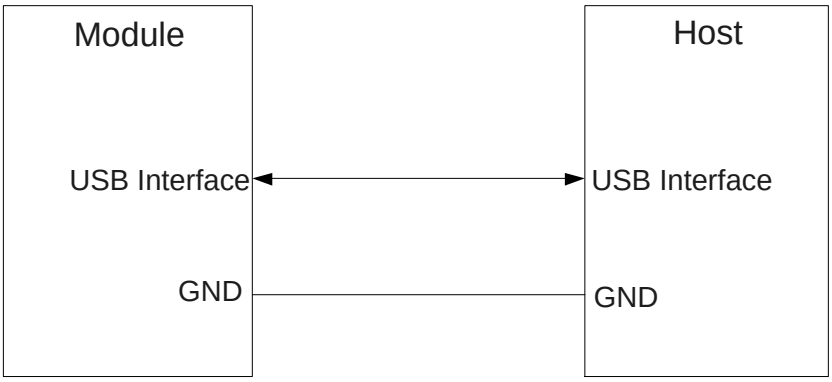


Figure 4: Sleep Mode Application with USB Remote Wakeup

The module and the host will wake up in the following conditions.

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, it will send remote wake-up signals via USB to wake up the host.

3.1.2. Airplane Mode

When the module enters airplane mode, the RF function does not work and all AT commands related to the RF function are inaccessible. The following ways can be used to let the module enter airplane mode.

Hardware:

The W_DISABLE# pin is pulled up by default. Its control function for airplane mode is disabled by default, and **AT+QCFG="airplanecontrol",1** can be used to enable the function. Driving the pin low after its control function for airplane mode is enabled by AT command can make the module enter the airplane mode.

Software:

AT+CFUN=<fun> provides the choice of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode (disable (U)SIM and RF functions).
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode (disable RF function).

NOTE

The execution of **AT+CFUN** will not affect GNSS function. For more details about the AT command, see ***document [4]***.

3.2. Communication Interface with a Host

The module supports to communicate through both USB and PCIe interfaces, respectively referring to the USB mode and the PCIe mode as described below.

USB Mode

- Supports all USB 2.0/3.1 features.
- Supports MBIM/QMI/QRTR/AT over USB interface.
- Communication can be switched to PCIe mode by AT command.

USB is the default communication interface between the module and the host. To use PCIe interface for the communication between a host, an AT command under USB mode can be used. For more details about the AT command, see ***document [4]***.

It is suggested that USB 2.0 interface be reserved for firmware upgrade.

USB-AT-based PCIe Mode

- Supports MBIM/QMI/QRTR/AT over PCIe interface.
- Supports AT over USB interface.
- Communication can be switched back to USB mode by AT command.

When the module works at the USB-AT-based (switched from USB mode by AT command) PCIe mode, it can be switched back to USB mode by **AT+QCFG= "data_interface",0,0**. For more details about the command, see ***document [4]***.

In USB-AT-based PCIe mode, the firmware upgrade via PCIe interface is not supported, so USB 2.0 interface must be reserved for the firmware upgrade.

eFuse-based PCIe Mode

- Supports MBIM/QMI/QRTR/AT over PCIe interface.
- Supports Non-X86 systems and X86 system (supports BIOS PCIe early initial).

In eFuse-based PCIe mode, the firmware upgrade via PCIe interface is supported. The module can also be reprogrammed to PCIe mode based on eFuse. If switched to PCIe mode by burnt eFuse, the communication cannot be switched back to USB mode.

Note that if the host does not support firmware upgrade through PCIe, the firmware can be upgraded by the 5G-M2 EVB, which could be connected to PC with a USB cable. For more details, see ***document [3]***.

3.3. Power Supply

3.3.1. Power Supply Interface

Table 8: Definition of VCC and GND Pins

Pin	Pin Name	I/O	Description	DC Characteristics
2, 4, 70, 72, 74	VCC	PI	Power supply for the module	Vmin = 3.135 V Vnom = 3.7 V

				Vmax = 4.4 V
3, 5, 11, 27, 33, 39, 45, 51, 57, 71	GND	-	Ground	-

3.3.2. Reference Design for Power Supply.

The power source is critical to the module's performance. The continuous current of the power supply should be 3 A at least and the peak current should be 4 A at least.

The following figure shows a reference design for +5.0 V input power source based on a DC-DC converter. The typical output of the power supply is 3.7 V.

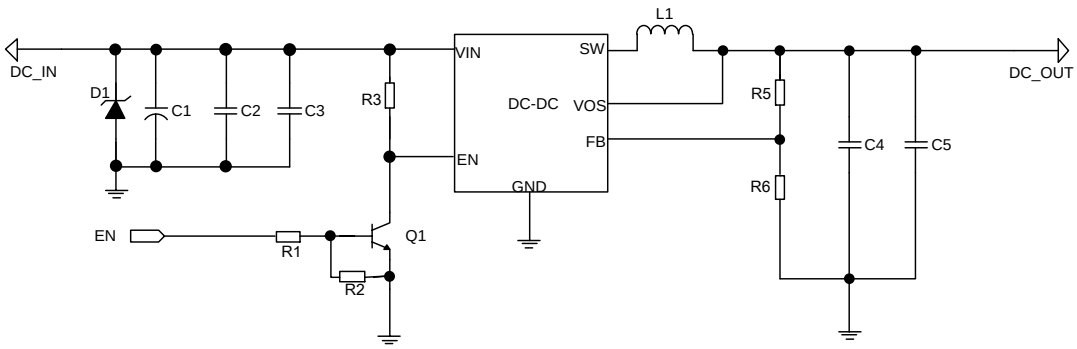


Figure 5: Reference Circuit for Power Supply

NOTE

To avoid corrupting the data in the internal flash, DO NOT cut off the power supply before the module is completely turned off by pulling down FULL_CARD_POWER_OFF# pin for more than 900 ms, and DON'T cut off power supply directly when the module is working.

3.3.3. Voltage Stability Requirements

The power supply range of the module is from 3.135 V to 4.4 V. Ensure that the input voltage never drops below 3.135 V, otherwise the module will power off automatically. The voltage ripple of the input power supply should be less than 100 mV. The figure below shows the power supply limits during burst transmission when 3.3 V power supply is applied.

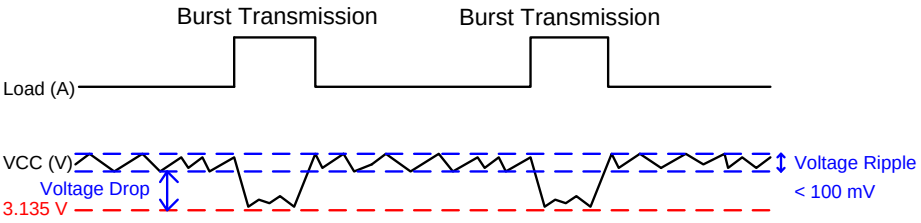


Figure 6: Power Supply Limits during Burst Transmission

To decrease the voltage drop, two bypass capacitors of 220 µF with low ESR should be used, and a multi-layer ceramic chip capacitor (MLCC) array should also be used due to its ultra-low ESR. It is recommended to use ceramic capacitors (100 nF, 6.8 nF, 220 pF, 68 pF, 15 pF, 9.1 pF, 4.7 pF) for composing the MLCC array, and place these capacitors close to VCC pins. The width of VCC trace should be not less than 3 mm. In principle, the longer the VCC trace is, the wider it should be.

In addition, to guarantee stability of the power supply, it is recommended to use a TVS with working peak reverse voltage of 5 V.

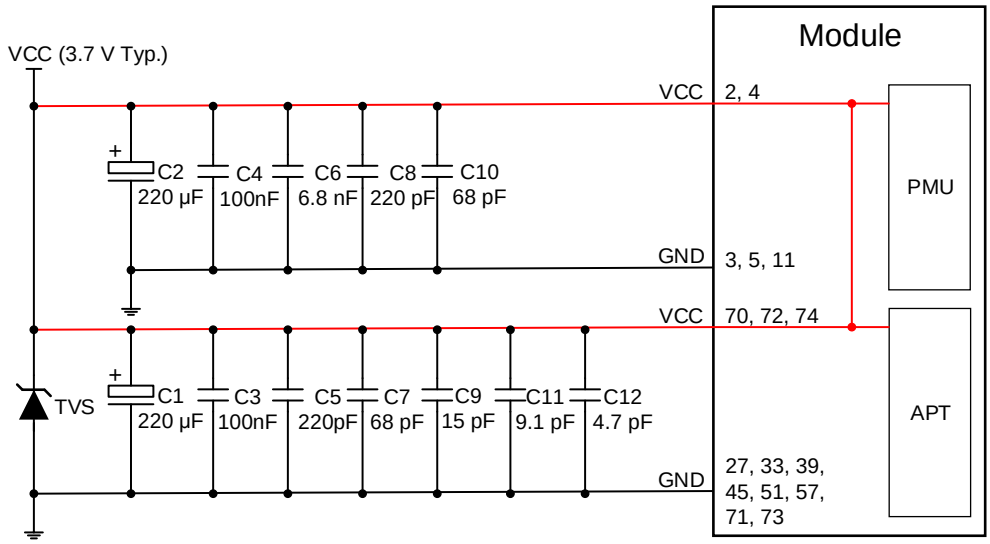


Figure 7: Reference Circuit for VCC

3.3.4. Power Supply Monitoring

AT+CBC can be used to monitor the voltage value of VCC. For more details about the AT command, see ***document [4]***.

3.4. Turn On

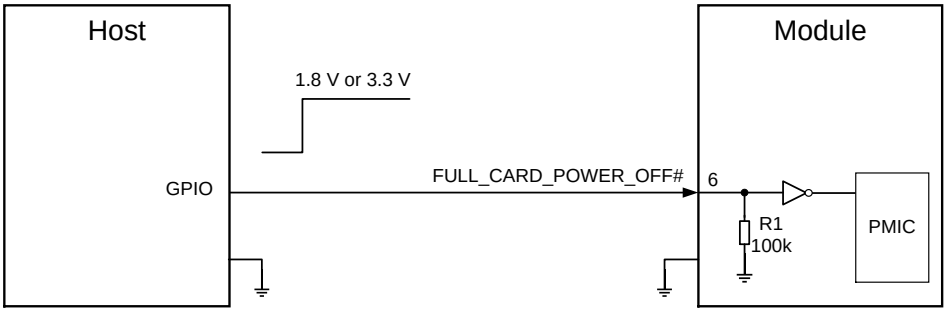
FULL_CARD_POWER_OFF# is used to turn on/off the module or reset the module through hard reset. This input signal is 3.3 V tolerant and can be driven by either 1.8 V or 3.3 V GPIO. And it has internally pulled down with a 100 kΩ resistor.

When FULL_CARD_POWER_OFF# is driven high (≥ 1.19 V), the module will turn on.

Table 9: Definition of FULL_CARD_POWER_OFF#

Pin No.	Pin Name	I/O	Description	DC Characteristics	Comment
6	FULL_CARD_ POWER_OFF#	DI	Turn on/off the module. High level: Turn on Low level: Turn off	V_{IH}max = 3.6 V V_{IH}min = 1.19 V V_{IL}max = 0.2 V	Pull down with a 100 kΩ resistor.

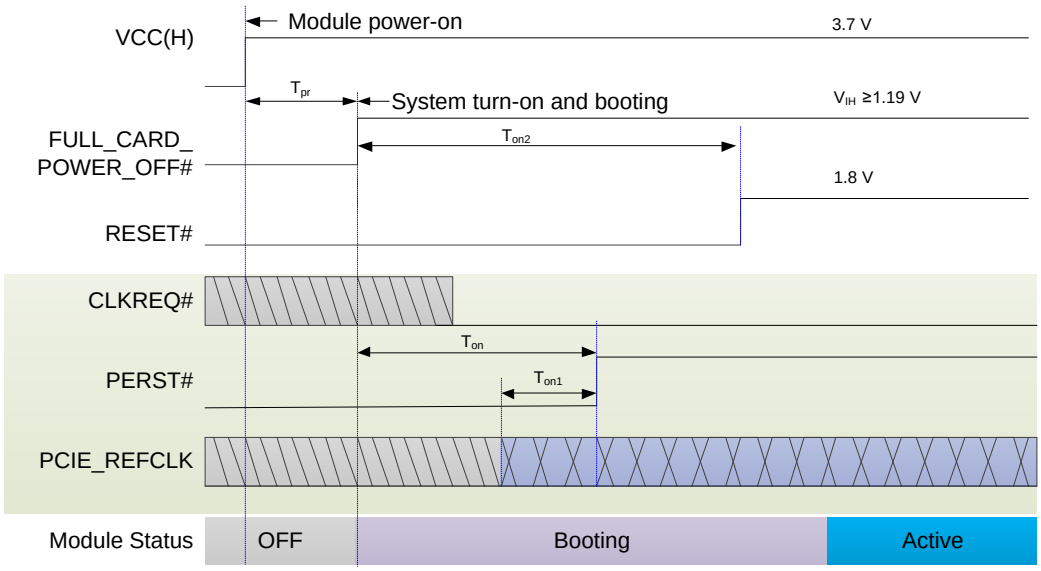
It is recommended to use a host GPIO to control FULL_CARD_POWER_OFF#. A simple reference circuit is illustrated by the following figure.



NOTE: The voltage of pin 6 should be not less than 1.19 V when it is at HIGH level.

Figure 8: Turn on the Module with a Host GPIO

The timing of turn-on scenario is illustrated by the following figure.



NOTE:
1. When the module is in USB mode, please ignore the PCIe related signals and their timing parameters in the figure.
2. During power-up stage, RESET# will be driven high internally and automatically without the host pulling down RESET#.

Figure 9: Turn-on Timing of the Module

Table 10: Turn-on Timing of the Module

Symbol	Min.	Typ.	Max.	Comment
T_{pr}	100 ms	-	-	The module's power-on time before system turn-on on and booting, which varies depending on the host.
T_{on}	100 ms	-	-	The period when the host GPIO controls the module to exit the PCIe reset state. 1. For eFuse-based PCIe mode, Min. T_{on} is 100 ms. 2. For USB-AT-based PCIe mode, Typ. T_{on} is 3 s.
	-	3 s	-	
T_{on1}	100 μs	-	-	The period during which PCIE_REFCLK_P/M is stable before PERST# is driven high.
T_{on2} [11]	TBD	-	-	The period from the host pulling up FULL_CARD_POWER_OFF# to the module pulling up RESET# internally and automatically.

NOTE

When the FULL_CARD_POWER_OFF# signal is low, please avoid any leakage current entering the module's DPR pin from the Host.

[11] At booting stage, the host must not drive RESET# low after FULL_CARD_POWER_OFF# is at high level.

For the laptop application scenario, there are two reset signals to control PERST# pin of the module, and the following figure is for reference. It is recommended that AUX Reset be pulled up before Global PCIe Reset is driven high.

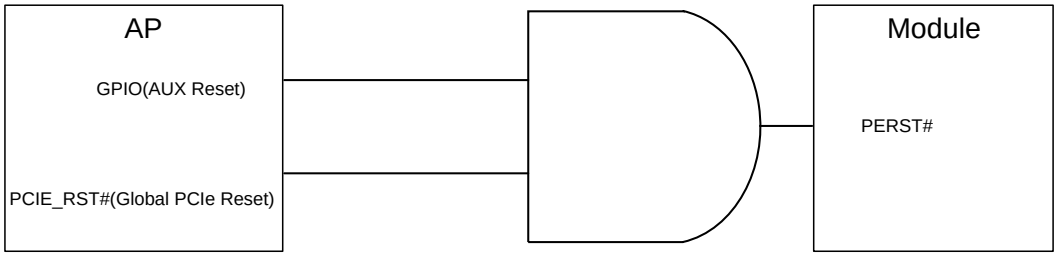
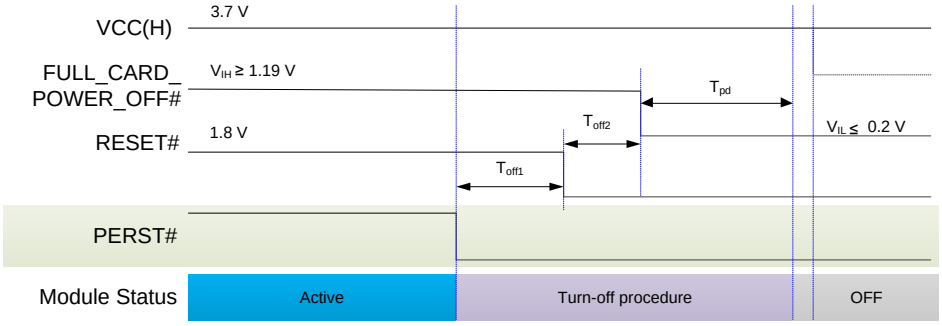


Figure 10: Reference Circuit for Laptop PCIe Reset Logic

3.5. Turn Off

For the design that turns on the module with a host GPIO, when the power is supplied to VCC, driving FULL_CARD_POWER_OFF# pin LOW (≤ 0.2 V) or tri-stating the pin will turn off the module.

The timing of turn-off scenario is illustrated by the following figure.



NOTE:
When the module is in USB mode, please ignore the PCIe related signals and their timing parameters in the figure.

Figure 11: Turn-off Timing through FULL_CARD_POWER_OFF#

Table 11: Turn-off Timing of the Module through FULL_CARD_POWER_OFF#

Symbol	Min.	Typ.	Max.	Comment
T_{off1}	-	100 ms	-	The period from the host pulling down PERST# to it pulling down RESET#.

T_{off2}	0 ms	100 ms	-	The period from the host pulling down RESET# to it pulling down FULL_CARD_POWER_OFF#.
T_{pd}	900 ms	-	-	The period from the host pulling down FULL_CARD_POWER_OFF# to the module turning off. It is recommended to cut off VCC when the module has been powered off completely.

3.6. Reset

RESET# is an active LOW signal (1.8 V logic level). When this pin is at low level, the module will immediately enter reset condition.

Please note that triggering the RESET# signal will lead to loss of all data in the module and removal of system drivers. It will also disconnect the modem from the network.

Table 12: Definition of RESET# Pin

Pin No.	Pin Name	I/O	Description	DC Characteristics	Comment
67	RESET#	DI	Reset the module. Active LOW	1.8 V	Internally pulled up to 1.8 V. A test point is recommended to be reserved if unused.

The module can be reset by pulling down the RESET#. An open collector/drain driver or a button can be used to control RESET#.

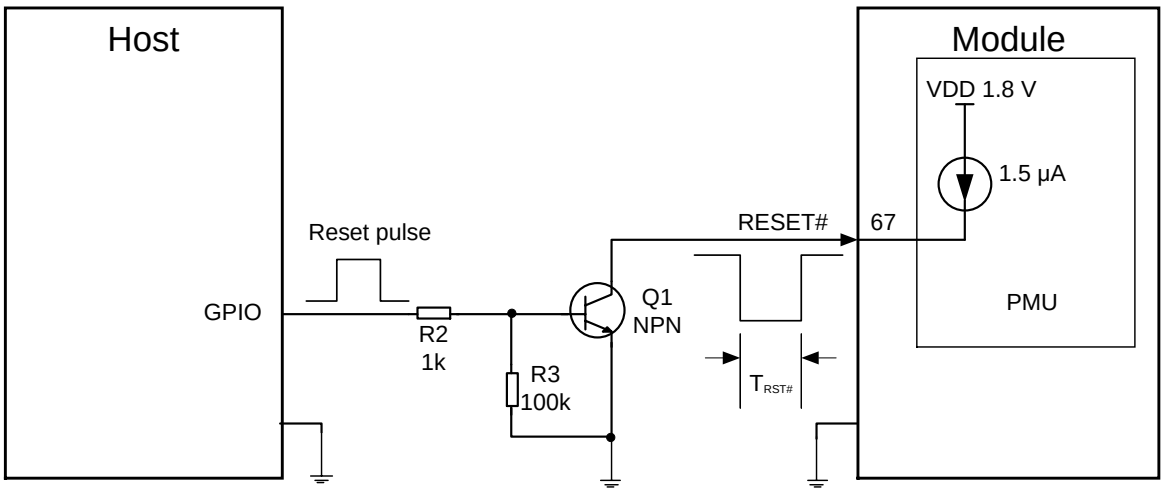


Figure 12: Reference Circuit for RESET# with NPN Driver Circuit

NOTE

The host's RESET#-controlling GPIO may cause an unexpected module reset during the host reset, so pay attention to the signal level of the host GPIO to avoid it.

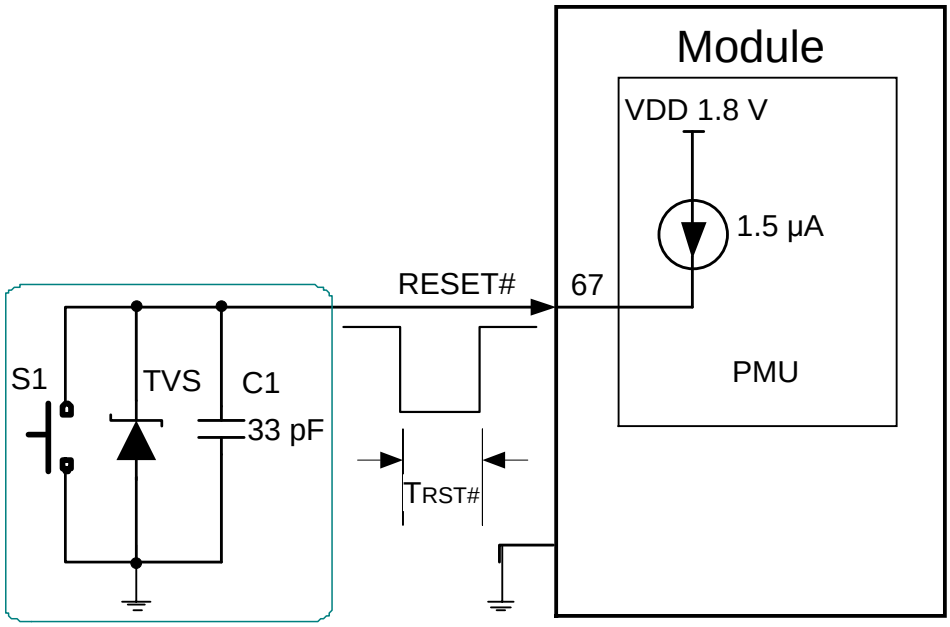
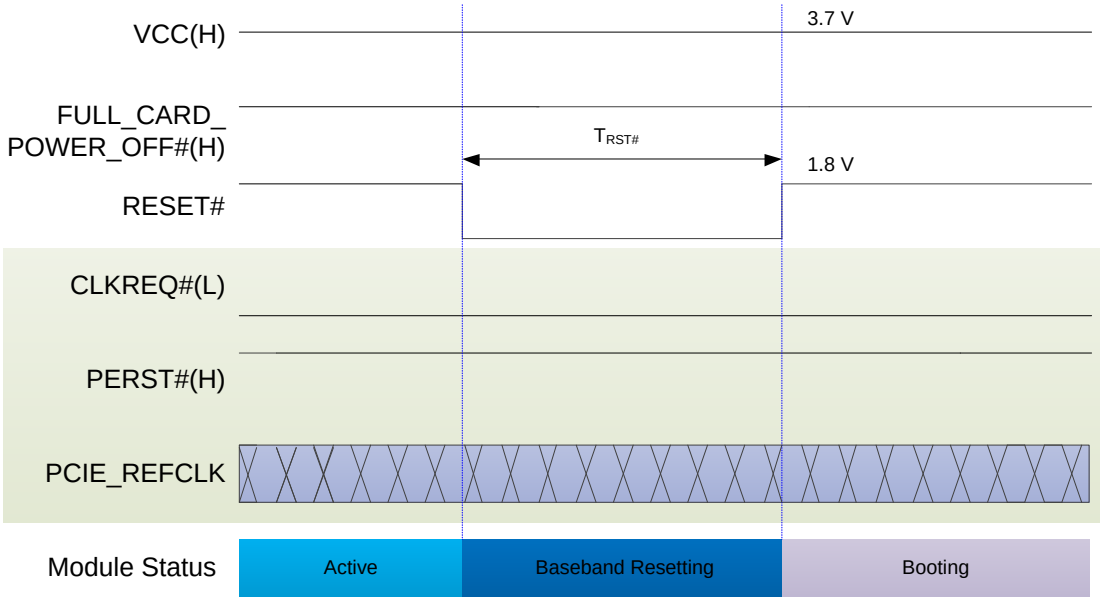


Figure 13: Reference Circuit for RESET# with a Button

For a warm reset when only the reset signal is pulled LOW, see the timing illustrated by the figure below. In this reset mode, the power of the module will not be turned off. This timing sequence is recommended for scenarios where the module is reset with a button.



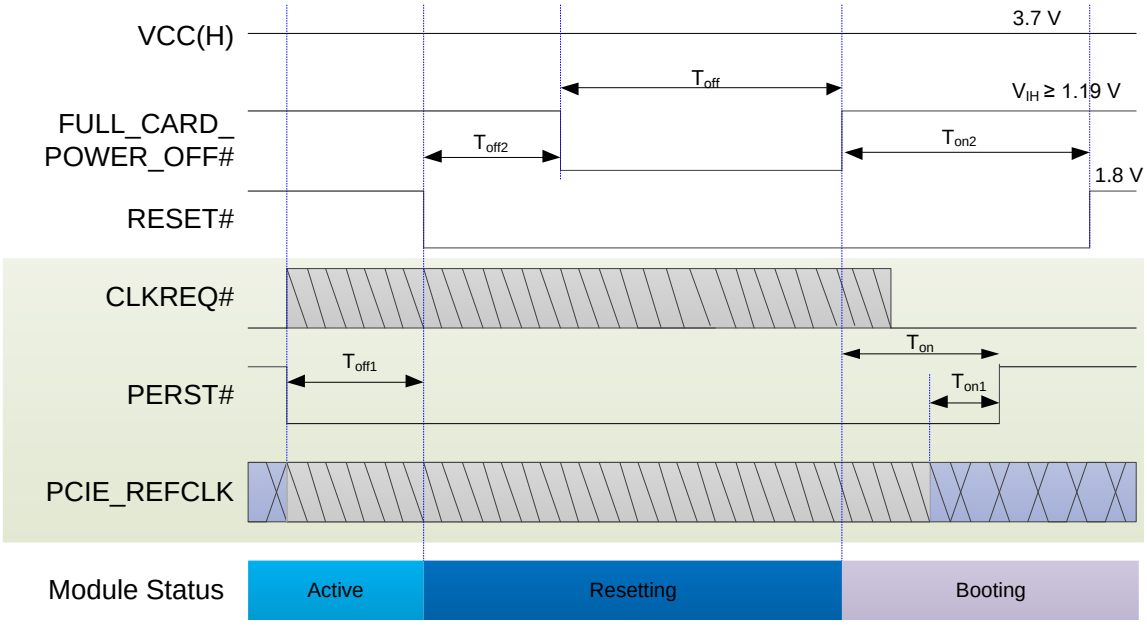
NOTE:
When the module is in USB mode, please ignore the PCIe related signals and their timing parameters in the figure.

Figure 14: Reset Timing of the Module's Warm Reset

Table 13: Reset Timing of the Module's Warm Reset

Symbol	Min.	Typ.	Max.	Comment
$T_{RST\#}$	200 ms	400 ms	-	Reset baseband chip IC only

For a hard reset, see the timing illustrated by the figure below. This timing sequence is recommended for scenarios where the module is reset with NPN driver circuit.



NOTE:
1. The timing parameters after the host pulls up FULL_CARD_POWER_OFF# refer to the boot timing of the PCIe mode module.
2. When the module is in USB mode, please ignore the PCIe related signals and their timing parameters in the figure.

Figure 15: Reset Timing of the Module's Hard Reset

Table 14: Reset Timing of the Module's Hard Reset

Symbol	Min.	Typ.	Max.	Comment
T_{off1}	-	100 ms	-	The period from the host pulling down PERST# to it pulling down RESET#.
T_{off2}	0 ms	100 ms	-	The period from the host pulling down RESET# to it pulling down FULL_CARD_POWER_OFF#.
T_{off}	900 ms	-	-	Module hard reset. The period that FULL_CARD_POWER_OFF is pulled low. Ensure that the module has been turned off completely.
T_{on}	100 ms	-	-	The period when the host GPIO controls the module to exit the PCIe reset state. 1. For eFuse-based PCIe mode, Min. T_{on} is 100 ms. 2. For USB-AT-based PCIe mode, Typ. T_{on} is 3 s.
	-	3 s	-	
T_{on1}	100 µs	-	-	The period during which PCIE_REFCLK_P/M is stable before PERST# is driven high.
T_{on2} [11]	TBD	-	-	The period from the host pulling up FULL_CARD_POWER_OFF# to the module pulling up RESET# internally and automatically.

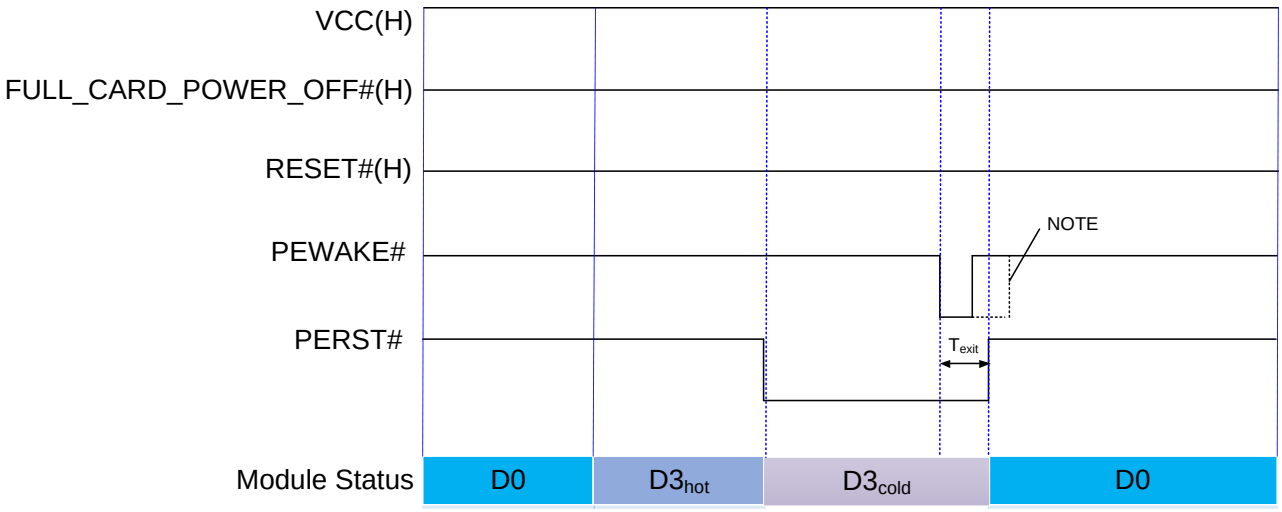
NOTE

When the FULL_CARD_POWER_OFF# signal is low, please avoid any leakage current entering the module's DPR pin from the host.

3.7. $D3_{cold}$ State

For the laptop application scenario, module must go through $D3_{hot}$ before entering $D3_{cold}$. In $D3_{hot}$ state, PERST# must be kept in high level.

The module enters $D3_{cold}$ state after PERST# is at low level. The module enters D0 state after PERST# is at high level.



NOTE: PEWAKE# may be pulled up before or after PERST# is pulled up, depending on when HOST pulls up PERST#. This time does not affect the normal operation of the module and can be ignored.

Figure 16: PCIe $D3_{cold}$ State Timing

Table 15: Exit $D3_{cold}$ State Timing of the Module

Symbol	Min.	Typ.	Max.	Comment
T_{exit}	50 ms	150 ms	500 ms	The period from the module pulling down PEWAKE# to HOST pulling up PERST#.

4 Application Interfaces

The physical connections and signal levels of the module comply with the PCI Express M.2 specification. This chapter mainly describes the definition and application of the following interfaces/pins of the module:

4.1. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 3.1 Gen 2 and USB 2.0 specifications and supports SuperSpeed (10 Gbps) on USB 3.1 and high-speed (480 Mbps) and full-speed (12 Mbps) modes on USB 2.0. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB*.

Table 16: Pin Definition of USB Interface

Pin No.	Pin Name	I/O	Description	Comment
7	USB_DP	AIO	USB differential data (+)	Require differential impedance of 90 Ω. Test points must be reserved.
9	USB_DM	AIO	USB differential data (-)	
29	USB_SS_TX_M	AO	USB 3.1 SuperSpeed transmit (-)	Require differential impedance of 90 Ω.
31	USB_SS_TX_P	AO	USB 3.1 SuperSpeed transmit (+)	
35	USB_SS_RX_M	AI	USB 3.1 SuperSpeed receive (-)	
37	USB_SS_RX_P	AI	USB 3.1 SuperSpeed receive (+)	

For more details about the USB 3.1 Gen 2 and 2.0 specifications, please visit http://www.usb.org/home.

The USB 2.0 interface is recommended to be reserved for firmware upgrade in designs. The following figure shows a reference circuit of USB interface.

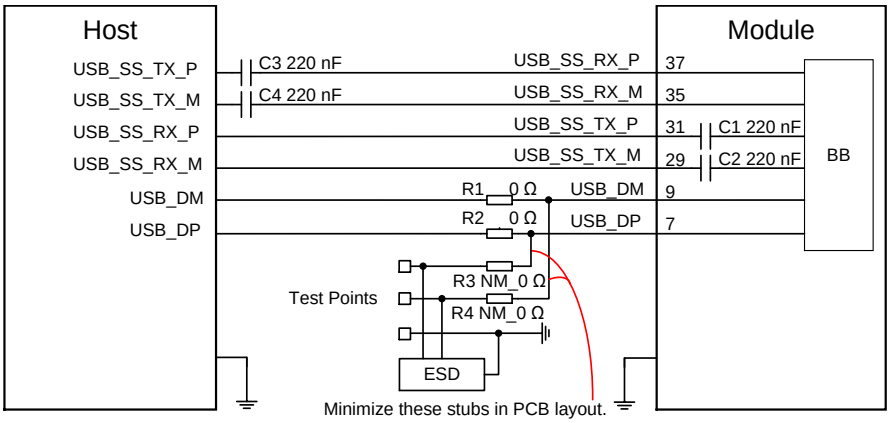


Figure 17: Reference Circuit of USB 3.1 & 2.0 Interface

AC coupling capacitors C3 and C4 must be placed close to the host and close to each other. C1 and C2 have been integrated inside the module, so do not place these two capacitors on your schematic and PCB. To ensure the signal integrity of USB 2.0 data traces, R1, R2, R3 and R4 must be placed close to the module, and the stubs must be minimized in PCB layout.

You should follow the principles below when designing for the USB interface to meet USB specifications.

- The impedance of differential trace of USB 2.0 and USB 3.1 should be 90 Ω.
- Route the USB signal traces as differential pairs in the inner layers of the PCB and surround the traces with ground on the same layer and with ground planes above and below. Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces.
- For USB 3.1 Gen 2 signal traces, the intra-pair length mismatch (P/M) should be less than 0.7 mm, while the inter-pair length mismatch (Tx/Rx) should be less than 10 mm.
- For USB 2.0 signal traces, the trace length should be less than 225 mm, and the intra-pair length matching (P/M) should be less than 2 mm.
- Junction capacitance of the ESD protection component might cause influences on USB data traces, so you should pay attention to the selection of the component. Typically, the stray capacitance should be less than 1.0 pF for USB 2.0, and less than 0.15 pF for USB 3.1 Gen 2.
- Keep the ESD protection components as close to the USB connector as possible.
- If possible, reserve 0 Ω resistors on USB_DP and USB_DM traces respectively.

4.2. (U)SIM Interfaces

The (U)SIM interface circuitry meets *ISO/IEC 7816-3,* ETSI and IMT-2000 requirements. Both Class B (3.0 V) and Class C (1.8 V) (U)SIM cards are supported.

4.2.1. Pin Definition of (U)SIM

The module has two (U)SIM interfaces, and supports dual SIM single standby.

Table 17: Pin Definition of (U)SIM Interfaces

Pin No.	Pin Name	I/O	Description	Comment
36	USIM1_VDD	PO	(U)SIM1 card power supply	USIM1_VDD 1.8/3.0 V
34	USIM1_DATA	DIO	(U)SIM1 card data	
32	USIM1_CLK	DO	(U)SIM1 card clock	
30	USIM1_RST	DO	(U)SIM1 card reset	
66	USIM1_DET [12]	DI	(U)SIM1 card hot-plug detect	1.8 V
48	USIM2_VDD	PO	(U)SIM2 card power supply	USIM2_VDD 1.8/3.0 V
42	USIM2_DATA	DIO	(U)SIM2 card data	
44	USIM2_CLK	DO	(U)SIM2 card clock	
46	USIM2_RST	DO	(U)SIM2 card reset	
40	USIM2_DET [12]	DI	(U)SIM2 card hot-plug detect	1.8 V

4.2.2. (U)SIM Hot-Plug

The module supports (U)SIM card hot-plug via the (U)SIM card hot-plug detect pins (USIM1_DET and USIM2_DET), which is disabled by default. (U)SIM card is detected by USIM_DET interrupt. (U)SIM card insertion is detected by high/low level.

USIM1_DET and USIM2_DET are pulled LOW by default, and will be internally pulled up to 1.8 V by software configuration only when (U)SIM hot-plug is enabled by **AT+QSIMDET**. Hot-plug function takes effect after the module is restarted. For more details about the AT command, see ***document [4]***.

The following command enables or disables (U)SIM card hot-plug function. The level of (U)SIM card detection pin should also be set when the (U)SIM card is inserted.

If the (U)SIM card connector doesn't support the hot-plug function, keep USIM_DET unconnected.

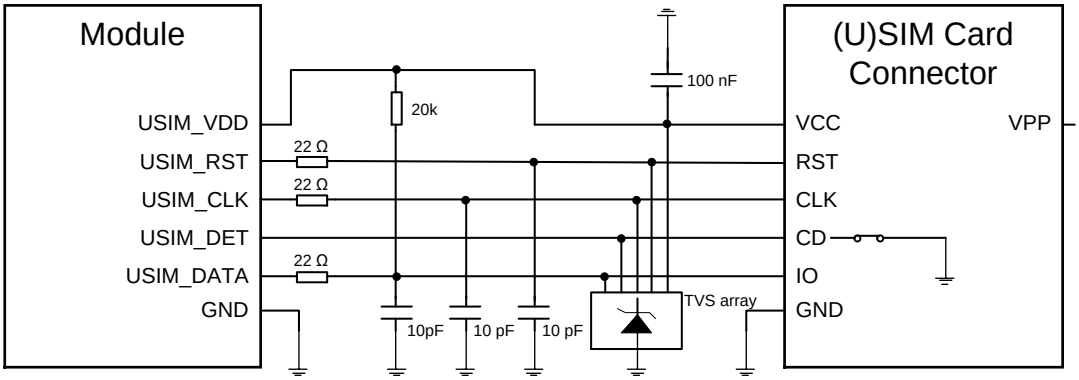
[12] USIM1_DET and USIM2_DET are pulled LOW by default, and will be internally pulled up to 1.8 V by software configuration only when (U)SIM hot-plug is enabled by **AT+QSIMDET**. Please do not add a pull-up resistor to USIM_DET pin.

4.2.3. Normally Closed (U)SIM Card Connector

With a normally closed (U)SIM card connector, USIM_DET pin is shorted to ground when there is no (U)SIM card inserted. (U)SIM card detection by high level is applicable to this type of connector. Once (U)SIM hot-plug is enabled by executing **AT+QSIMDET=1,1**, a (U)SIM card insertion will drive USIM_DET from low to high level, and the removal of it will drive USIM_DET from high to low level.

- When the (U)SIM is absent, CD is shorted to ground and USIM_DET is at low level.
- When the (U)SIM is present, CD is open from ground and USIM_DET is at high level.

The following figure shows a reference design for (U)SIM interface with a normally closed (U)SIM card connector.



NOTE: All these resistors, capacitors and TVS should be close to (U)SIM card connector in PCB layout.

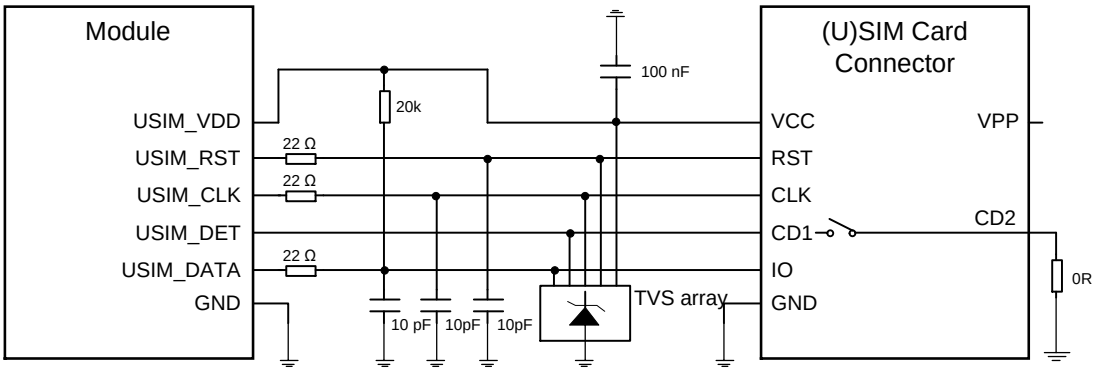
Figure 18: Reference Circuit for Normally Closed (U)SIM Card Connector

4.2.4. Normally Open (U)SIM Card Connector

With a normally open (U)SIM card connector, CD1 and CD2 of the connector are disconnected when there is no (U)SIM card inserted. (U)SIM card detection by low level is applicable to this type of connector. Once (U)SIM hot-plug is enabled by executing **AT+QSIMDET=1,0**, a (U)SIM card insertion will drive USIM_DET from high to low level, and the removal of it will drive USIM_DET from low to high level.

- When the (U)SIM is absent, CD1 is open from CD2 and USIM_DET is at high level.
- When the (U)SIM is present, CD1 is pull down to ground and USIM_DET is at low level.

The following figure shows a reference design for (U)SIM interface with a normally open (U)SIM card connector.



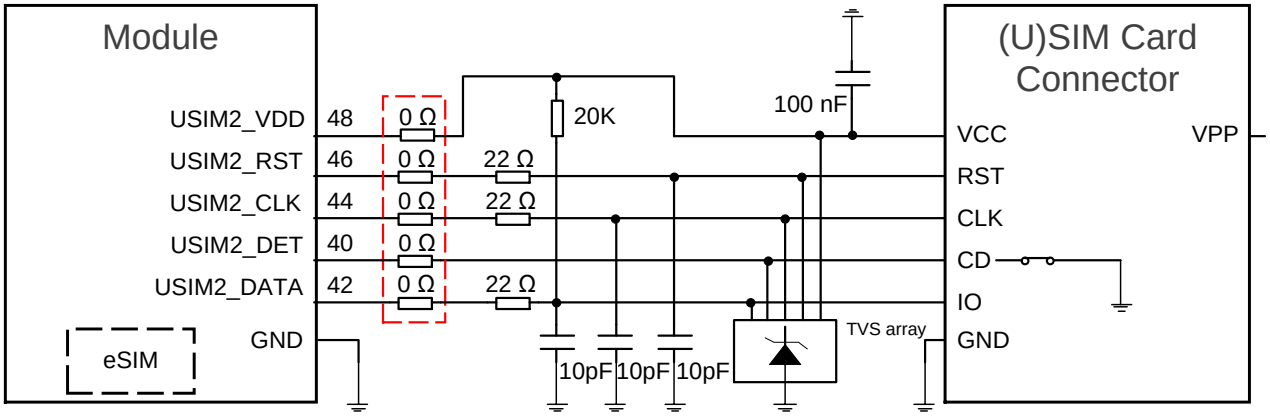
NOTE: All these resistors, capacitors and TVS should be close to (U)SIM card connector in PCB layout.

Figure 19: Reference Circuit for Normally Open (U)SIM Card Connector

4.2.5. (U)SIM2 Card Compatible Design

It should be noted that when the (U)SIM2 interface is used for an external (U)SIM card, the circuits are the same as those of (U)SIM1 interface. When the (U)SIM2 interface is used for the optional internal eSIM card, pins 40, 42, 44, 46 and 48 of the module must be kept open.

A recommended compatible design for the (U)SIM2 interface is shown below.



NOTE:
The five 0 Ω resistors must be placed close to the module, and all other components should be placed close to (U)SIM card connector in PCB layout.

Figure 20: Recommended Compatible Design for (U)SIM2 Interface

4.2.6. (U)SIM Design Notices

To enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design.

- Place the (U)SIM card connector as close to the module as possible, (U)SIM card related resistors, capacitors and ESD protection components should be placed close to the card connector. Keep the trace length as short as possible, less than 200 mm.
- Keep (U)SIM card signals away from RF and VCC traces.
- Keep the trace width of USIM_VDD at least 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer better ESD protection, add a TVS array of which the parasitic capacitance should be not higher than 10 pF. Add 22 Ω resistors in series between the module and the (U)SIM card connector to suppress EMI and enhance ESD protection. The 10 pF capacitors are used to filter out RF interference.
- For USIM_DATA, it is optional to add a 20 kΩ pull-up resistor near the (U)SIM card connector.

4.3. PCIe Interface

The module has one PCIe interface. Key features of the PCIe interface are as below:

- Compliant with *PCI Express Base Specification Revision 4.0*
- Supports RC and EP modes, EP mode by default
- Data rate: 8 Gbps/lane

It can be used to connect to an external Ethernet IC (MAC and PHY) or Wi-Fi IC.

4.3.1. Pin Definition of PCIe

The following table shows the pin definition of PCIe interface.

Table 18: Pin Definition of PCIe Interface

Pin No.	Pin Name	I/O	Description	Comment
55	PCIE_REFCLK_P	AIO	PCIe reference clock (+)	100 MHz. Require differential impedance of 85 Ω.
53	PCIE_REFCLK_M	AIO	PCIe reference clock (-)	
49	PCIE_RX_P	AI	PCIe receive (+)	Require differential impedance of 85 Ω.
47	PCIE_RX_M	AI	PCIe receive (-)	
43	PCIE_TX_P	AO	PCIe transmit (+)	Require differential impedance of 85 Ω.
41	PCIE_TX_M	AO	PCIe transmit (-)	

50	PERST#	DI [13]	PCIe reset Active LOW	1.8/3.3 V
52	CLKREQ#	OD [13]	PCIe clock request Active LOW	1.8/3.3 V
54	PEWAKE#	OD [13]	PCIe wake up Active LOW	1.8/3.3 V

4.3.2. Reference Design for PCIe

The following figure shows a reference circuit for the PCIe interface.

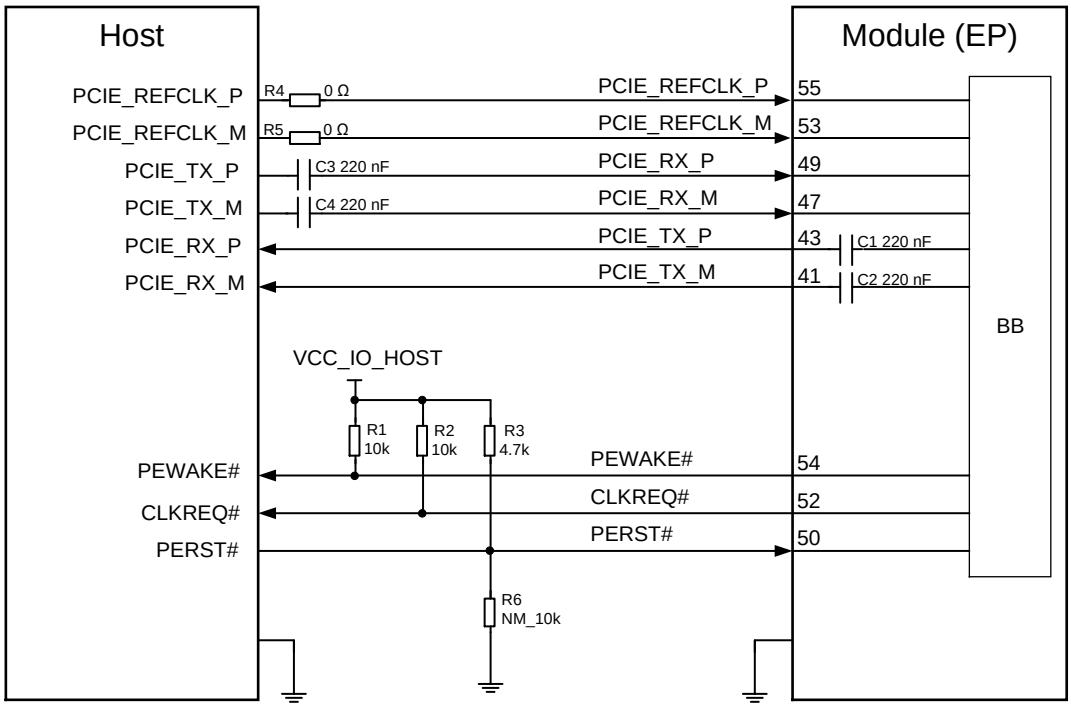


Figure 21: PCIe Interface Reference Circuit

To ensure the PCIe interface design meets PCIe Gen 3 specifications, you should follow the principles below:

- The differential impedance should be 85 Ω ±10 %.
- Route PCIe signal traces (Tx/Rx/REFCLK) as differential pairs with surrounded ground.
- For PCIe signal traces, the recommended maximum length for Tx and Rx differential data pairs should be less than 200 mm, and the intra-lane length mismatch of Tx and Rx differential data pairs should be less than 0.7 mm.

[13] PERST# behaves as DI in PCIe EP mode, and as OD in PCIe RC mode. CLKREQ# and PEWAKE# behave as OD in PCIe EP mode, and as DI in PCIe RC mode. PCIe EP mode is the default.

- To ensure the signal integrity of PCIe interface, AC coupling capacitors C3 and C4 should be placed close to the host on PCB. C1 and C2 have been integrated inside the module, so do not place these two capacitors on your schematic and PCB.
- Route PCIe differential signal traces at the inner-layer of PCB, and surround the traces with ground on that layer and with ground planes above and below Meanwhile, protect them from interferences such as crystal-oscillators, VBAT traces, RF signal traces.
- It is recommended to use a PUSH-PULL GPIO to output a low level that approaches to 0 V rather than using a pull-down resistor to get a low level. Otherwise, voltage division may be formed with the pull-up resistor inside the module, resulting in an uncertain 0 V voltage that could further lead to unpredictable problems. If host uses a push-pull GPIO to control PERST#, R3 can be not mounted.

4.4. Control and Indication Interfaces

The following table shows the pin definition of control and indication pins.

Table 19: Pin Definition of Control and Indication Interfaces

Pin No.	Pin Name	I/O	Description	DC Characteristics	Comment
8	W_DISABLE1#	DI	Airplane mode control Active LOW	1.8/3.3 V	
26	W_DISABLE2#	DI	GNSS control Active LOW	1.8/3.3 V	
10	LED_WWAN#	OD	RF status LED indicator Active LOW	VCC	-
23	WAKE_ON_ WAN#	OD	Wake up the host Active LOW	1.8 V	-
25	DPR	DI	Dynamic power reduction	1.8 V	-

4.4.1. W_DISABLE1#

The module provides a W_DISABLE1# pin to disable or enable airplane mode through hardware operation. W_DISABLE1# is pulled up by default. Driving it LOW will set the module to airplane mode. In airplane mode, the RF function will be disabled.

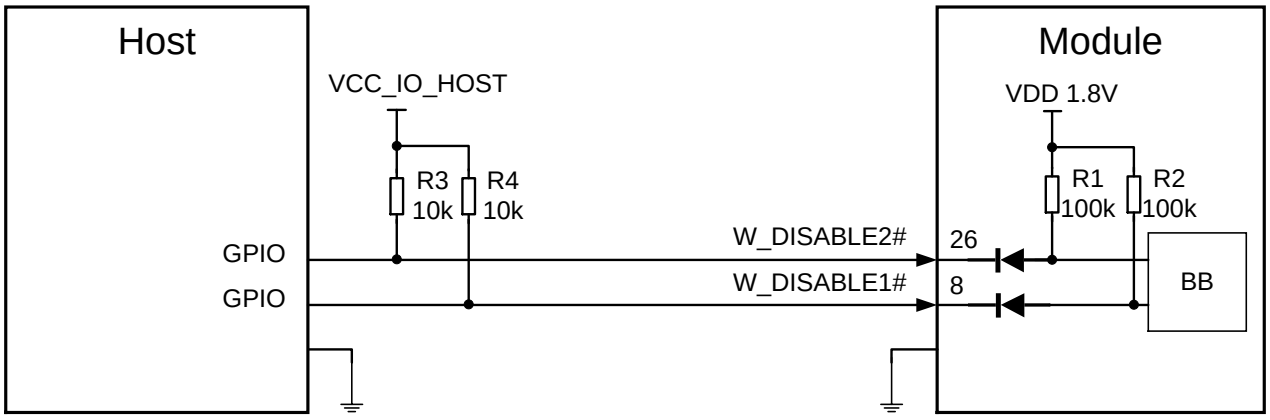
4.4.2. W_DISABLE2#*

The module provides a W_DISABLE2# pin to disable or enable the GNSS function. The W_DISABLE2# pin is pulled up by default. Driving it LOW will disable the GNSS function. The combination of W_DISABLE2# pin and AT commands can control the GNSS function. For details about the AT commands, see ***document [5]***.

Table 20: GNSS Function Status

W_DISABLE2# Logic Level	AT Commands	GNSS Function Status
High Level	**AT+QGPS=1**	Enabled
	AT+QGPSEND	Disabled
Low Level	**AT+QGPS=1**	Disabled
	AT+QGPSEND	

W_DISABLE1# and W_DISABLE2# are active LOW signals, and a reference circuit is shown as below.



NOTE: The voltage level of VCC_IO_HOST could be 1.8 V or 3.3 V typically.

Figure 22: W_DISABLE1# and W_DISABLE2# Reference Circuit

4.4.3. LED_WWAN#

LED_WWAN# is used to indicate the RF status of the module, and its sink current is up to 10 mA.

To reduce current consumption of the LED, a current-limited resistor must be placed in series with the LED, as illustrated in the figure below. The LED is ON when the LED_WWAN# signal is at low level.

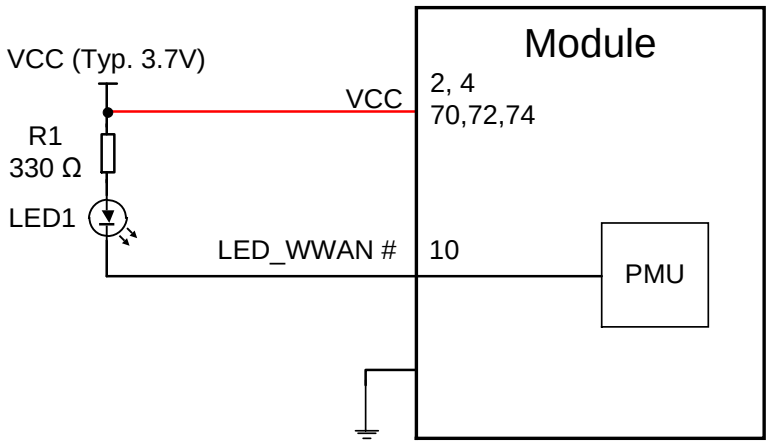


Figure 23: LED_WWAN# Reference Circuit

Table 21: Network Status Indications of LED_WWAN#

LED_WWAN# Logic Level	Description
Low Level (LED on)	RF function is turned on.
High Level (LED off)	RF function is turned off if any of the following occurs: ● The (U)SIM card is not powered. ● W_DISABLE1# is at low level (airplane mode enabled). ● **AT+CFUN=4** (RF function disabled).

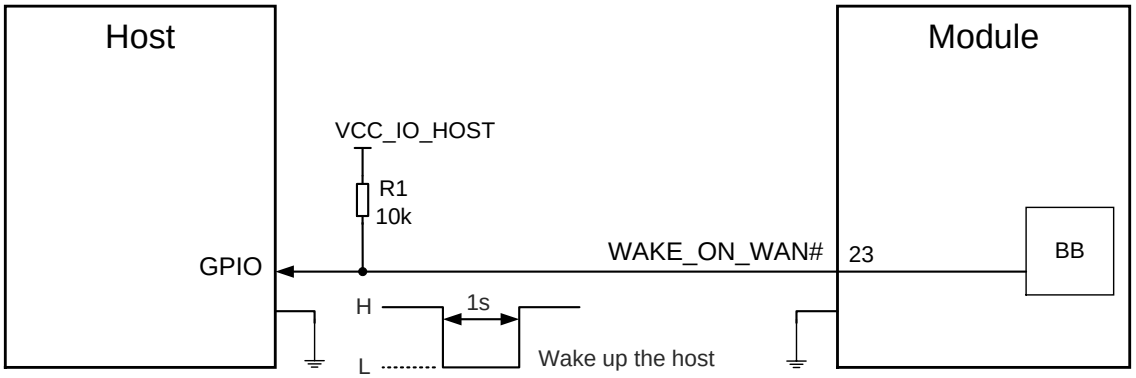
4.4.4. WAKE_ON_WAN#

The WAKE_ON_WAN# is an open drain pin, which requires a pull-up resistor on the host. When a URC returns, a one-second low level pulse signal will be outputted to wake up the host.

Table 22: State of the WAKE_ON_WAN#

WAKE_ON_WAN# State	Module Operation Status
Outputs a one-second pulse signal at low level	Call/SMS/Data is incoming (to wake up the host)

Always at high level	Idle/Sleep



NOTE:
The voltage level on VCC_IO_HOST depends on the host side due to the open drain in pin 23.

Figure 24: WAKE_ON_WAN# Signal Reference Circuit

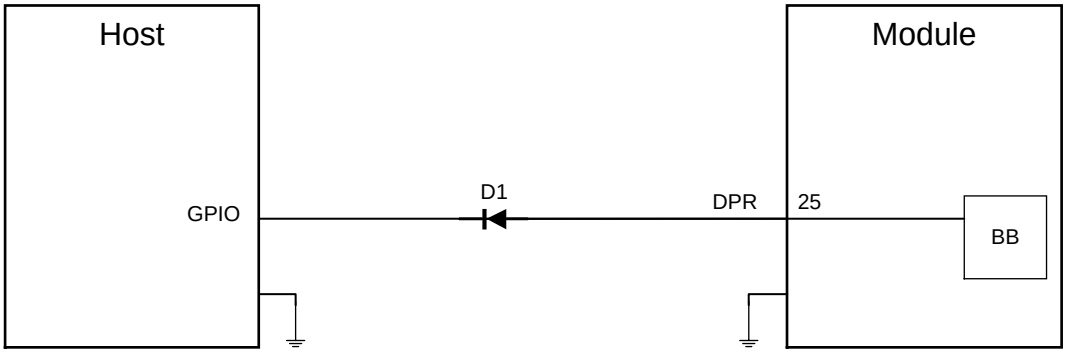
4.4.5. DPR

The module provides the DPR (Dynamic Power Reduction) pin for body SAR (Specific Absorption Rate) detection. The signal is sent from the proximity sensor of the host system to the module to provide an input trigger, which will reduce the output power in radio transmission.

Table 23: Function of the DPR Signal

DPR Level	Function
HIGH/Floating	NO maximum transmitting power backoff
LOW	Maximum transmitting power backoff by **AT+QSAR**

A reference circuit is shown as below.



NOTE:
Do not add pull-up resistor to DPR pin on the module side.

Figure 25: DPR Reference Circuit

NOTE

See ***document [6]*** for more details about **AT+QSAR**.

4.5. WWAN&WLAN Coexistence Interface

The module provides the WWAN&WLAN coexistence interface, the following table shows the pin definition of this interface.

Table 24: Pin Definition of COEX Interface

Pin No.	Pin Name	I/O	Description	DC Characteristics
60	N79_TX_EN*	DO	Notification from SDR to WLAN when n79 transmitting	1.8 V
38	WLAN_TX_EN*	DI	Notification from WLAN to SDR when WLAN transmitting	1.8 V
62	COEX_RXD [14]	DI	5G/LTE and WLAN coexistence receive	1.8 V
64	COEX_TXD [16]	DO	5G/LTE and WLAN coexistence transmit	1.8 V

[14] Please note that COEX_RXD and COEX_TXD cannot be used as general UART ports.

4.6. Configuration Pins

Configuration pins are used to assist the host to identify the presence of the module in the socket and identify module type. The module provides four configuration pins, which are defined as below.

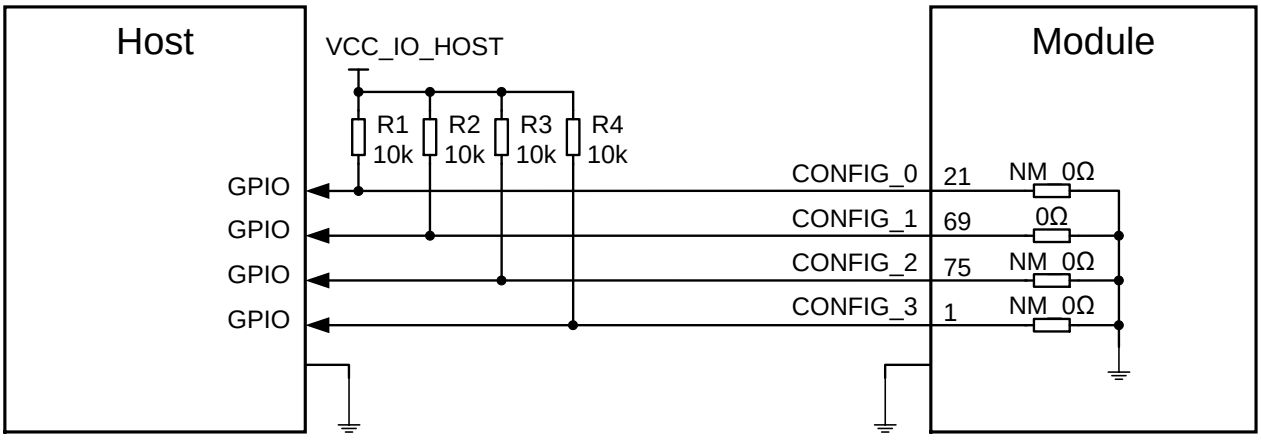
Table 25: Configuration Pins List of M.2 Specification

CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Module Type and Main Host Interface	Port Configuration
NC	GND	NC	NC	WWAN-PCIe, USB 3.1	2 (Quectel defined)

Table 26: Configuration Pins of the Module

Pin No.	Pin Name	I/O	Description
21	CONFIG_0	DO	Not connected internally
69	CONFIG_1	DO	Connected to GND internally
75	CONFIG_2	DO	Not connected internally
1	CONFIG_3	DO	Not connected internally

The following figure shows a reference circuit of these four pins.



NOTE: The voltage level of VCC_IO_HOST depends on the host side and could be 1.8 V or 3.3 V.

Figure 26: Recommended Circuit for Configuration Pins

5 RF Characteristics

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

This chapter mainly describes RF characteristics of the module. The module provides four antenna interfaces ANT0, ANT1, ANT2 and ANT3 and the impedance of them is 50 Ω.

5.1. mmWave IF Interfaces

5.1.1. Pin Definition

Six mmWave IF interfaces are provided to support NR FR2 (mmWave) bands n257, n258, n260, and n261. The following table lists the definition of these mmWave IF interfaces.

Table 27: Pin Definition of mmWave IF Interfaces

mmWave IF Interface	I/O	Functional Description
IFH1	AIO	Horizontal polarization IF output signal and control signal for mmWave RFIC device 2
IFH2	AIO	Horizontal polarization IF output signal and control signal for mmWave RFIC device 1
IFV3	AIO	Vertical polarization IF output signal and LO signal for mmWave RFIC device 0
IFV1	AIO	Vertical polarization IF output signal and LO signal for mmWave RFIC device 2
IFV2	AIO	Vertical polarization IF output signal and LO signal for mmWave RFIC device 1
IFV3	AIO	Vertical polarization IF output signal and LO signal for mmWave RFIC device 0

For more details about reference circuit of mmWave IF interfaces, see ***document*** *错误!未找到引用源。*.

5.1.2. Port Mapping

RM551E-GL supports QTM545 (power class 3), and the IF port mapping is shown as below.

Table 28: RM530N-GL mmWave IF Port Mapping

QTM_PON	RM530N-GL mmWave IF Port	QTM545
QTM0_PON	IFH3	QTM545-0_IF(H)
	IFV3	QTM545-0_IF(V)
QTM1_PON	IFH2	QTM545-1_IF(H)
	IFV2	QTM545-1_IF(V)
QTM2_PON	IFH1	QTM545-2_IF(H)
	IFV1	QTM545-2_IF(V)

5.2. Sub-6 GHz & GNSS Antenna Interfaces

5.2.1. Pin Definition

The pin definition of antenna interfaces is shown below.

Table 29: RM551E-GL Pin Definition of Antenna Interfaces

Pin Name	I/O	Description	LB (MHz)	MHB (MHz)	n77/n78 (MHz)	n79 (MHz)	LAA (MHz)
ANT0	AIO	**5G NR:** - Reframing: LB TX /PRX & MHB TX0 /PRX & UHB TX1/DRX - n41 TX0/PRX - n77/n78/n79 TX1/DRX **LTE:** LB TX/PRX & MHB TX0/PRX & UHB TX1/DRX **WCDMA:** LMB TRX	617–960	1427–2690	3300–4200	4400–5000	-
ANT1	AIO	**5G NR:** - Reframing: MHB PRX MIMO & UHB PRX MIMO - n41 PRX MIMO - n77/n78/n79 PRX MIMO **LTE:** MHB PRX MIMO & UHB PRX MIMO & LAA PRX **GNSS:** L5	617–960	1427–2690	3300–4200	4400–5000	5150-5925
ANT2	AIO	**5G NR:** - Reframing: MHB TX1 [15]/ DRX MIMO & UHB TX0/PRX - n41 TX1/DRX MIMO	617–960	1427–2690	3300–4200	4400–5000	-

[15] MHB TX1 will be active when supporting Sub 2.6 GHz EN-DC.

		- n77/n78/n79 TX0/PRX **LTE:** MHB TX1 [17]/DRX MIMO & UHB TX0/PRX					
ANT3	AIO	**5G NR:** - Refarming: LB DRX & MHB DRX & UHB DRX MIMO - n41 DRX - n77/n78/n79 DRX MIMO **LTE:** LB DRX & MHB DRX & UHB DRX MIMO & LAA DRX **WCDMA:** LMB DRX **GNSS:** L1	617–960	1427–2690	3300–4200	4400–5000	5150-5925

5.2.2. Cellular Network

5.2.2.1. Rx Sensitivity

Table 30: RM551E-GL Conducted Receiving Sensitivity (Unit: dBm)

Mode	Frequency	Primary	Diversity	SIMO [16]	3GPP (SIMO)
WCDMA	WCDMA B1	TBD	TBD	TBD	TBD
	WCDMA B2	TBD	TBD	TBD	TBD
	WCDMA B4	TBD	TBD	TBD	TBD
	WCDMA B5	TBD	TBD	TBD	TBD
	WCDMA B8	TBD	TBD	TBD	TBD
	WCDMA B19	TBD	TBD	TBD	TBD
LTE	LTE-FDD B1 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-FDD B2 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-FDD B3 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-FDD B4 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-FDD B5 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-FDD B7 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-FDD B8 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-FDD B12 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-FDD B13 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-FDD B14 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-FDD B17 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-FDD B18 (10 MHz)	TBD	TBD	TBD	TBD

[16] For the SIMO receiving sensitivity, WCDMA bands, LTE bands and 5G n5/n8/n12/n13/n14/n18/n20/n26/n28/n71/n75/n76 are tested with 2 Rx antennas, and 5G n1/n2/n3/n7/n25/n30/n38/n40/n41/n48/n66/n70/n77/n78/n79 are tested with 4 Rx antennas.

	LTE-FDD B19 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-FDD B20 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-FDD B25 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-FDD B26 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-FDD B28 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-FDD B29 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-FDD B30 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-FDD B32 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-TDD B34 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-TDD B38 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-TDD B39 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-TDD B40 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-TDD B41 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-TDD B42 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-TDD B43 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-TDD B46 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-TDD B48 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-FDD B66 (10 MHz)	TBD	TBD	TBD	TBD
	LTE-FDD B71 (10 MHz)	TBD	TBD	TBD	TBD
5G NR	5G NR-FDD n1 (20 MHz)	TBD	TBD	TBD	TBD
	5G NR-FDD n2 (20 MHz)	TBD	TBD	TBD	TBD
	5G NR-FDD n3 (20 MHz)	TBD	TBD	TBD	TBD
	5G NR-FDD n5 (20 MHz)	TBD	TBD	TBD	TBD
	5G NR-FDD n7 (20 MHz)	TBD	TBD	TBD	TBD
	5G NR-FDD n8 (20 MHz)	TBD	TBD	TBD	TBD

5G NR-FDD n12 (15 MHz)	TBD	TBD	TBD	TBD
5G NR-FDD n13 (10MHz)	TBD	TBD	TBD	TBD
5G NR-FDD n14 (10 MHz)	TBD	TBD	TBD	TBD
5G NR-FDD n18 (15 MHz)	TBD	TBD	TBD	TBD
5G NR-FDD n20 (20 MHz)	TBD	TBD	TBD	TBD
5G NR-FDD n25 (20 MHz)	TBD	TBD	TBD	TBD
5G NR-FDD n26 (20 MHz)	TBD	TBD	TBD	TBD
5G NR-FDD n28 (20 MHz)	TBD	TBD	TBD	TBD
5G NR-FDD n29 (10 MHz)	TBD	TBD	TBD	TBD
5G NR-FDD n30 (10 MHz)	TBD	TBD	TBD	TBD
5G NR-TDD n38 (20 MHz)	TBD	TBD	TBD	TBD
5G NR-TDD n40 (20 MHz)	TBD	TBD	TBD	TBD
5G NR-TDD n41 (100 MHz)	TBD	TBD	TBD	TBD
5G NR-TDD n48 (20 MHz)	TBD	TBD	TBD	TBD
5G NR-FDD n66 (40 MHz)	TBD	TBD	TBD	TBD
5G NR-FDD n70 (20 MHz)	TBD	TBD	TBD	TBD
5G NR-FDD n71 (20 MHz)	TBD	TBD	TBD	TBD
5G NR-SDL n75 (20 MHz)	TBD	TBD	TBD	TBD
5G NR-SDL n76 (5 MHz)	TBD	TBD	TBD	TBD
5G NR-TDD n77 (100 MHz)	TBD	TBD	TBD	TBD
5G NR-TDD n78 (100 MHz)	TBD	TBD	TBD	TBD
5G NR-TDD n79 (100 MHz)	TBD	TBD	TBD	TBD

5.2.2.2. Tx Power

The following table shows the RF output power of the module.

Table 31: RM551E-GL Cellular Output Power

Mode	Frequency	Max.	Min.
WCDMA	WCDMA bands	23 dBm ±2 dB (Class 3)	< -50 dBm
LTE	LTE bands	23 dBm ±2 dB (Class 3)	< -40 dBm
	LTE HPUE bands (B38/B41/B42/B43)	26 dBm ±2 dB (Class 2) [17]	< -40 dBm
5G NR	5G NR bands	23 dBm ±2 dB (Class 3)	< -40 dBm [18]
	5G NR HPUE bands (n38/n40/n41/n77/n78/n79)	26 dBm +2/-3 dB (Class 2) [19]	< -40 dBm [20]
	5G NR HPUE bands (n41/n77/n78/n79)	29 dBm +1/-2(Class 1.5) [19]	< -40 dBm [18]

5.2.3. GNSS (Optional)

The module includes a fully integrated global navigation satellite system solution (GPS, GLONASS, BDS, Galileo and QZSS).

The module supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1 Hz data update rate via USB interface by default.

The GNSS engine is switched off by default, and it has to be switched on via AT command. For more details on GNSS positioning technology and configuration, see ***document [5]***.

5.2.3.1. GNSS Frequency

Table 32: GNSS Frequency

Bands	Type	Frequency	Unit
L1	GPS/Galileo/QZSS	1575.42 ±1.023 (L1)	MHz
	Galileo	1575.42 ±2.046 (E1)	MHz
	QZSS	1575.42 (L1)	MHz
	GLONASS	1597.5–1605.8	MHz

[17] PC2 and PC1.5 are not available in Japan due to the local regulations.
[18] For 5G NR TDD bands, the normative reference for this requirement is *TS 38.101-1 clause 6.3.1.*

	BDS	1561.098 ±2.046	MHz
L5	GPS/Galileo/QZSS	1176.45 ±10.23 (GPS L5)	MHz

5.2.3.2. GNSS Performance

The following table shows GNSS performance of the module.

Table 33: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity	Acquisition	Autonomous	TBD	dBm
	Reacquisition	Autonomous	TBD	dBm
	Tracking	Autonomous	TBD	dBm
TTFF	Cold start @ open sky	Autonomous	TBD	s
		XTRA enabled	TBD	s
	Warm start @ open sky	Autonomous	TBD	s
		XTRA enabled	TBD	s
	Hot start @ open sky	Autonomous	TBD	s
		XTRA enabled	TBD	s
Accuracy	CEP-50	Autonomous @ open sky	TBD	m

NOTE

1. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).

5.3. Antenna Tuner Control Interface

RFFE interface are used for antenna tuner control and should be routed to an appropriate antenna control circuit.

Table 34: Pin Definition of Antenna Tuner Control Interface

Pin No.	Pin Name	I/O	Description	DC Characteristics
56	RFFE_CLK*	DO	Used for external MIPI IC control	1.8 V
58	RFFE_DATA*	DIO		1.8 V
24	VDDIO_1V8	PO	Provide 1.8 V for external circuit	1.8 V Max. output current: 50 mA

NOTE

If RFFE function is required, please contact Quectel for more details.

5.4. Antenna Connectors

5.4.1. Antenna Connector Specifications

5.4.1.1. mmWave IF Connectors

The dimensions of antenna receptacle (ECT: 818025398) on the RM551E-GL and plug (ECT: 818025399) are illustrated by the following figure.

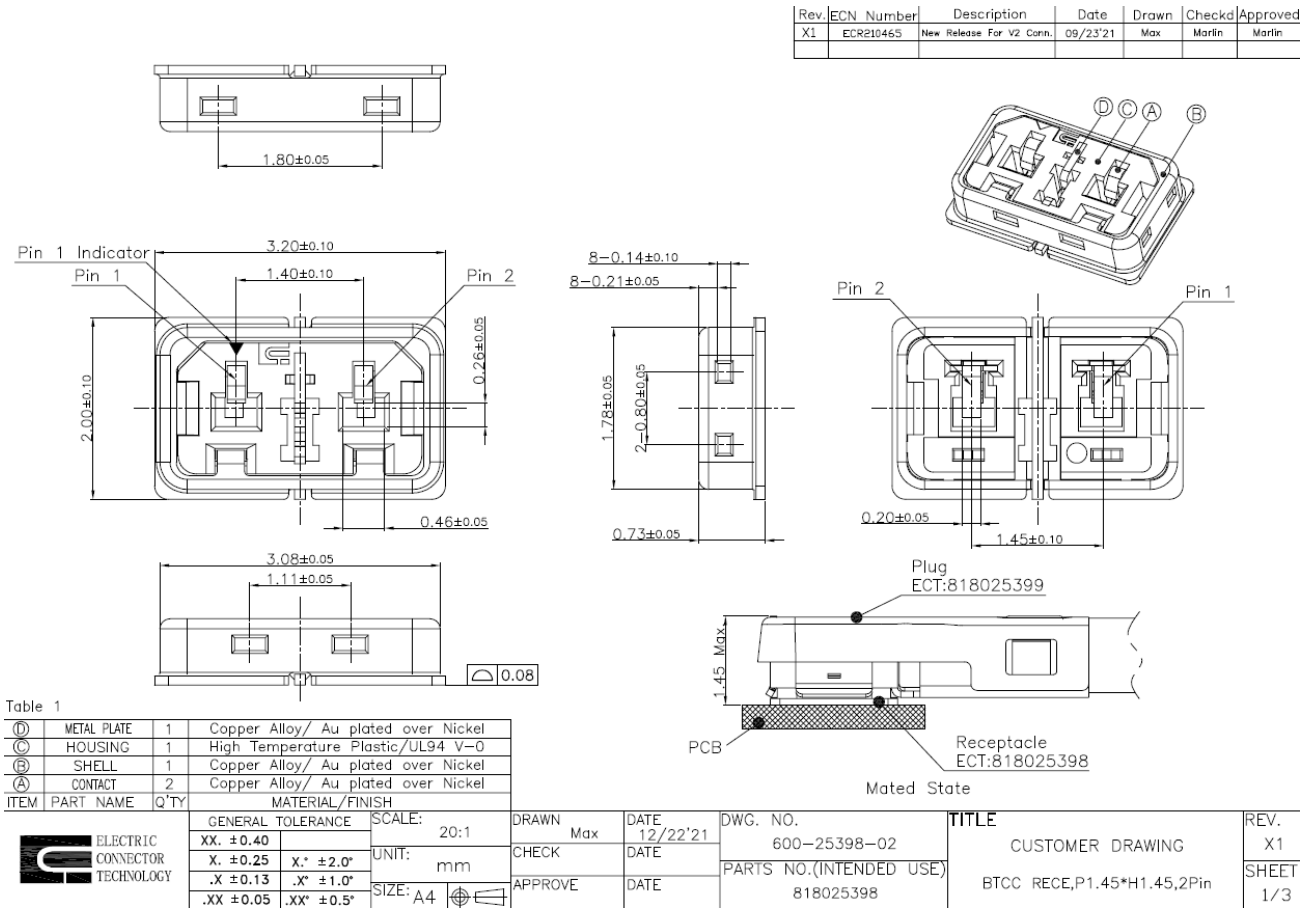


Figure 27: mmWave RF Connector Dimensions (Unit: mm)

5.4.1.2. Sub-6 GHz & GNSS Antenna Connectors

The module is mounted with standard 2 mm × 2 mm receptacle antenna connectors for convenient antenna connection. The antenna connector dimensions are illustrated as below:

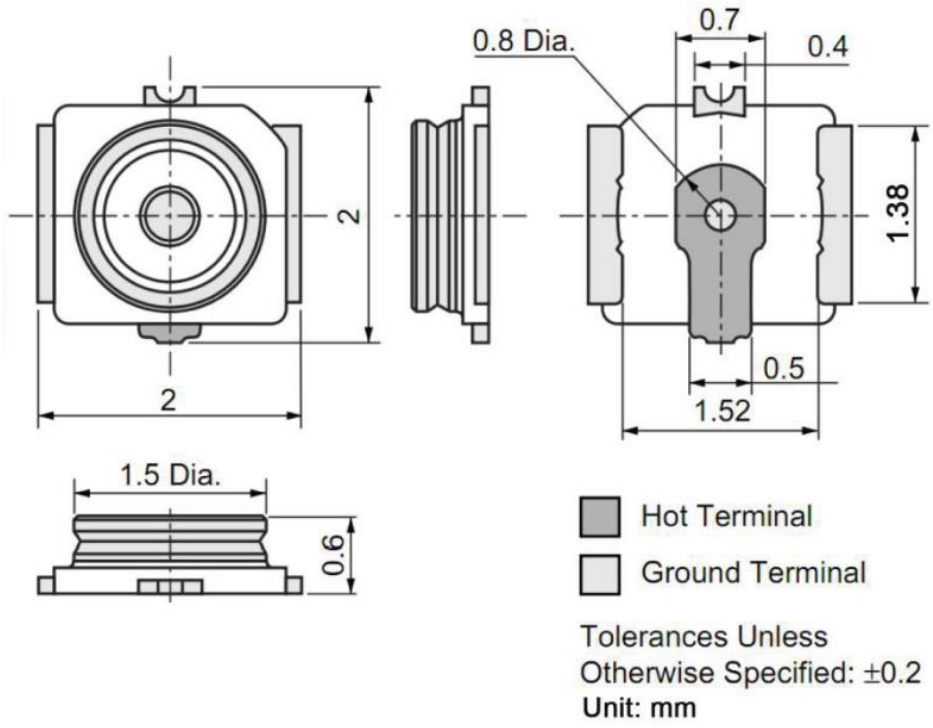


Figure 28: Dimensions of the Receptacle (Unit: mm)

Table 35: Major Specifications of the RF Connector

Item	Specification
Nominal Frequency Range	DC to 6 GHz
Nominal Impedance	50 Ω
Temperature Rating	-40 °C to +85 °C
Voltage Standing Wave Ratio (VSWR)	Meet the requirements of: Max 1.3 (DC–3 GHz) Max 1.4 (3–6 GHz)

5.4.2. Antenna Connector Location

RM551E-GL has six mmWave IF connectors (IFH1, IFV1, IFH2, IFV2, IFH3, IFV3), and four antenna connectors: ANT0, ANT1, ANT2 and ANT3, which are shown as below.

Figure 29: RM551E-GL Antenna Connectors

NOTE

It is recommended that the straight-line distance between the antenna and the module be greater than 15 mm to achieve better wireless performance of the whole device.

5.4.3. Antenna Connector Installation

The receptacle RF connector used in conjunction with the module will accept two types of mating plugs that will meet a maximum height of 1.2 mm using a Ø 0.81 mm coaxial cable or a maximum height of 1.45 mm utilizing a Ø 1.13 mm coaxial cable.

The following figure shows the specifications of mated plugs using Ø 0.81 mm coaxial cables.

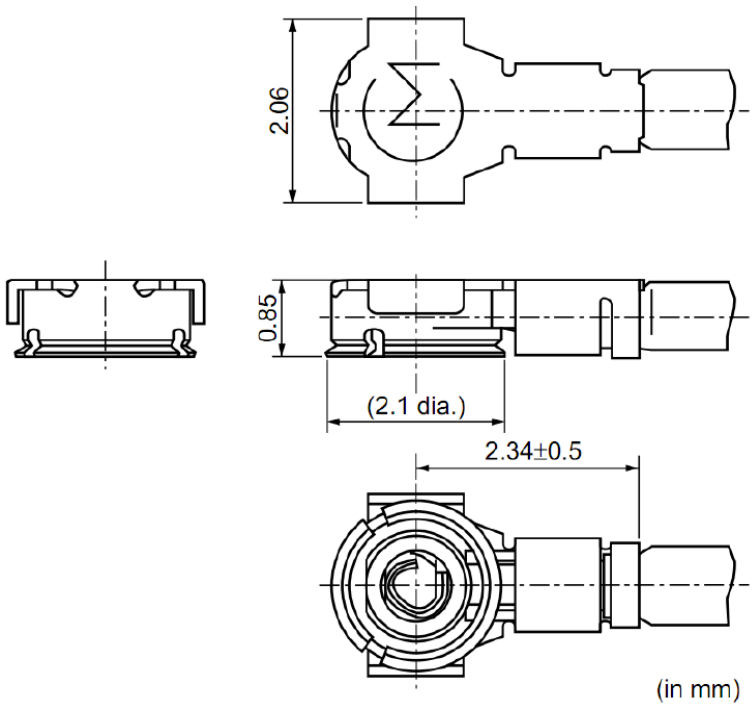


Figure 30: Dimensions of Mated Plugs (Ø0.81 mm Coaxial Cables) (Unit: mm)

The following figure illustrates the connection between the receptacle RF connector on the module and the mated plug using a Ø 0.81 mm coaxial cable.

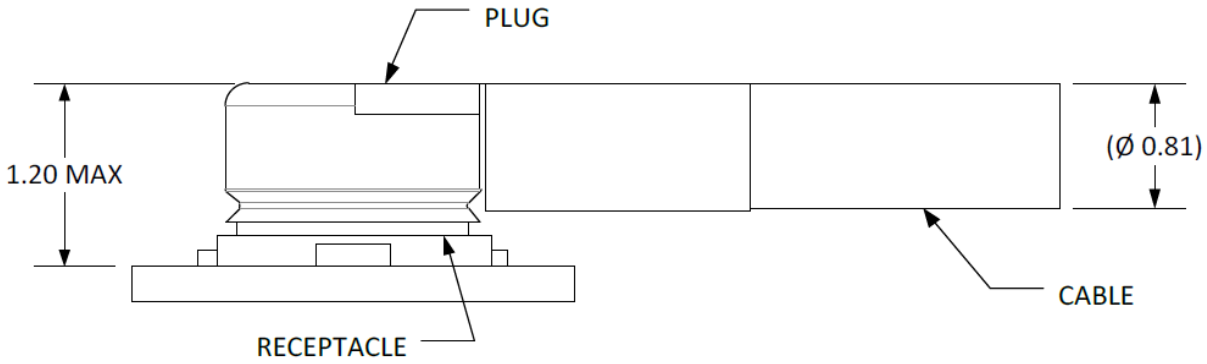


Figure 31: Space Factor of Mated Connectors (Ø0.81 mm Coaxial Cables) (Unit: mm)

The following figure illustrates the connection between the receptacle RF connector on the module and the mated plug using a Ø 1.13 mm coaxial cable.

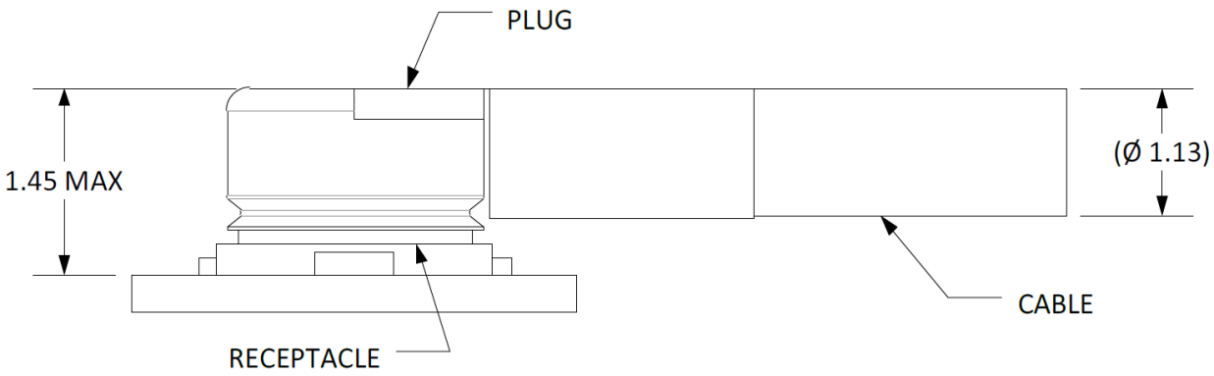


Figure 32: Space Factor of Mated Connectors (Ø 1.13 mm Coaxial Cables) (Unit: mm)

5.4.4. Recommended RF Connector Installation

5.4.4.1. Assemble Coaxial Cable Plug Manually

The illustration for plugging in a coaxial cable plug is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

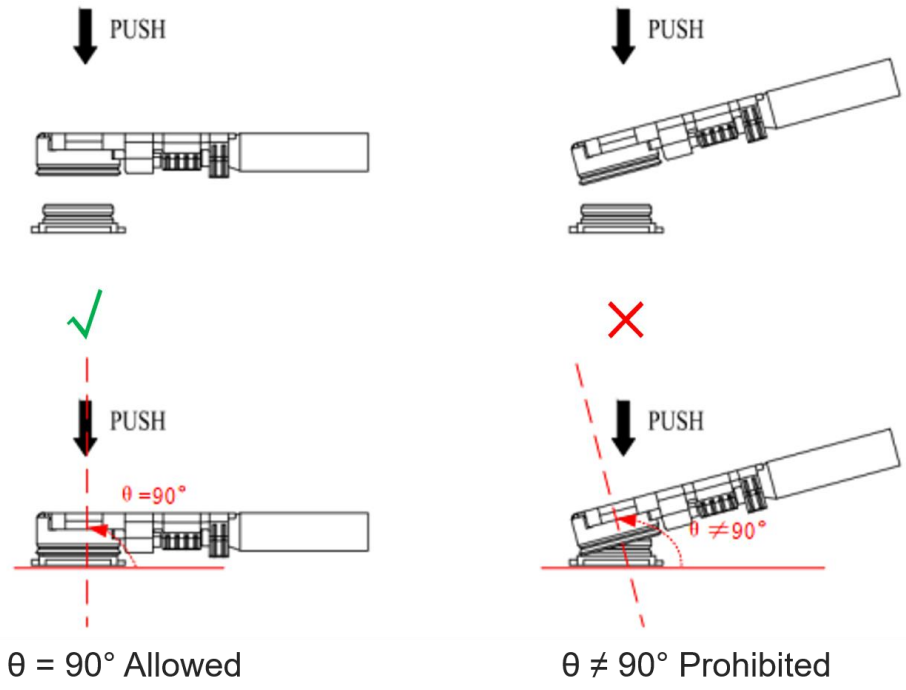


Figure 33: Plug in a Coaxial Cable Plug

The illustration of pulling out the coaxial cable plug is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

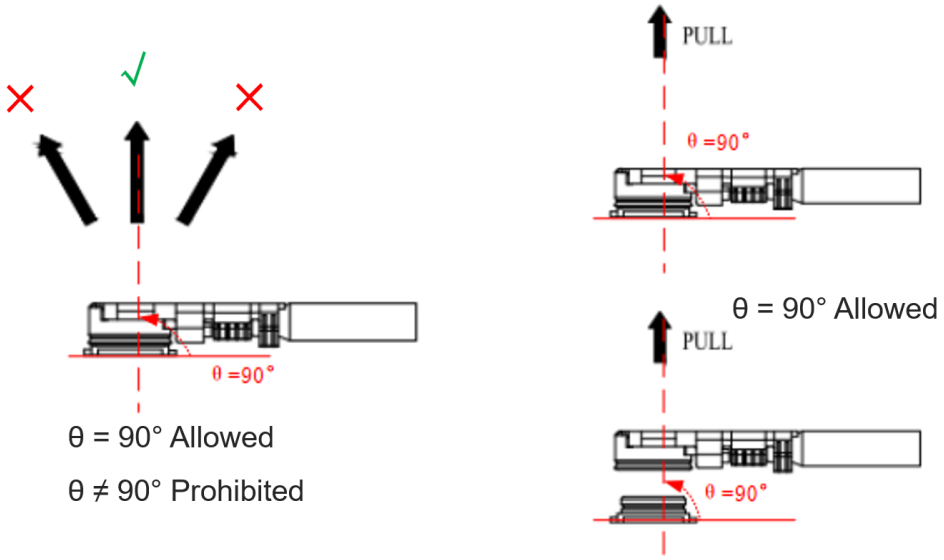


Figure 34: Pull out a Coaxial Cable Plug

5.4.4.2. Assemble Coaxial Cable Plug with Jig

The pictures of installing the coaxial cable plug with a jig is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

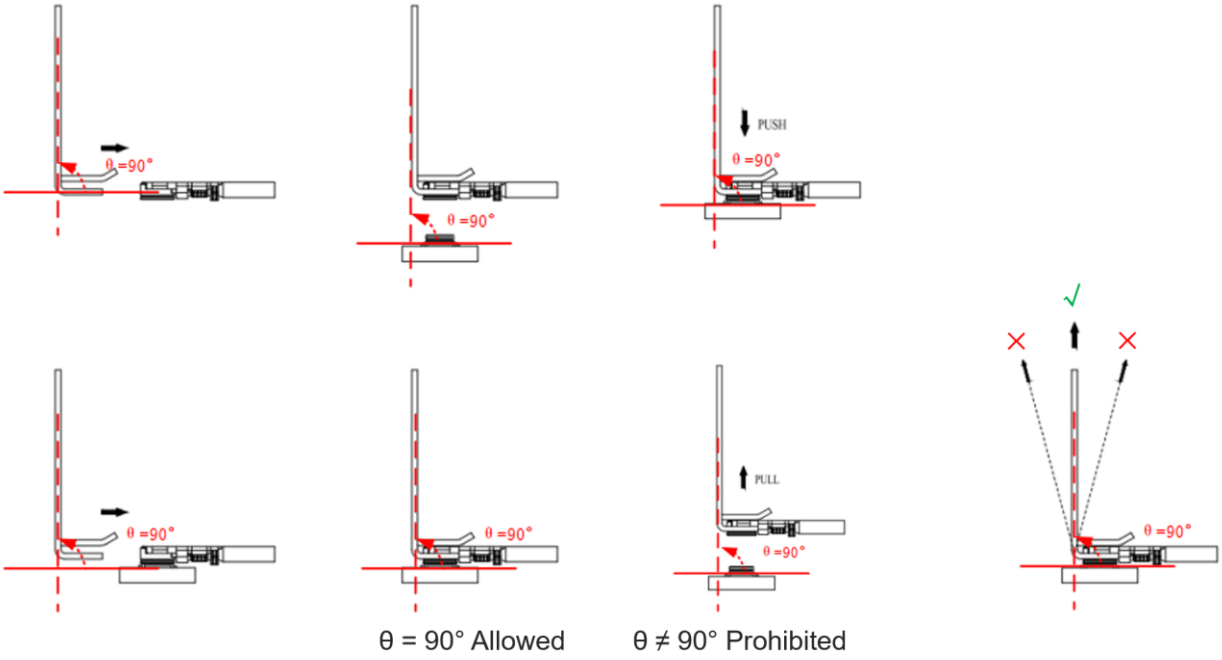


Figure 35: Install the Coaxial Cable Plug with Jig

5.4.5. Recommended Manufacturers of RF Connector and Cable

RF connectors and cables by I-PEX are recommended. For more details, visit https://www.i-pex.com.

5.5. Antenna Requirements

The following table shows the requirements on WCDMA, LTE, 5G NR antenna and GNSS antennas.

Table 36: Antenna Requirements

Type	Requirements
WCDMA/LTE/5G NR	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Input Impedance: 50 Ω ● Cable insertion loss: - < 1 dB: LB (<1 GHz) - < 1.5 dB: MB (1–2.3 GHz) - < 2 dB: HB (> 2.3 GHz)
GNSS	● Frequency range: L1: 1559–1609 MHz L5: 1166–1187 MHz ● Polarization: RHCP or linear ● VSWR: ≤ 2 (Typ.) ● Passive antenna gain: > 0 dBi

NOTE

It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 37: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VCC	-0.3	4.7	V
Voltage at 1.8 V Digital Pins	-0.3	2.3	V
Voltage at 3.3 V Digital Pins	-0.3	3.6	V

6.2. Power Supply Requirements

The typical input voltage of the module is 3.7 V, the following table shows the power supply requirements of the module.

Table 38: Power Supply Requirements

Parameter	Description	Min.	Typ.	Max.	Unit
VCC	Power Supply	3.135	3.7	4.4	V
Voltage Ripple	-	-	30	100	mV

6.3. Power Consumption

Table 39: Averaged Current Consumption for RM551E-GL

Mode	Conditions	Band/Combinations	Typ.	Unit
Power-off	Power off	-	TBD	μA
Sleep State	**AT+CFUN=0** (USB 3.1 suspended)	-	TBD	mA
	AT+CFUN=4 (USB 3.1 suspended)	-	TBD	mA
	SA FDD PF = 64 (USB 3.1 suspended)	-	TBD	mA
	SA TDD PF = 64 (USB 3.1 suspended)	-	TBD	mA
Idle State	SA PF = 64 (USB 2.0 active)	-	TBD	mA
	SA PF = 64 (USB 3.1 active)	-	TBD	mA
LTE	LTE LB @ 24 dBm	B5	TBD	mA
	LTE MB @ 24 dBm	B1	TBD	mA
	LTE HB @ 24 dBm	B7	TBD	mA
LTE CA	DL 3CA, 256QAM	CA_1A-3A-7A	TBD	mA
	UL 1CA, 256QAM			
	Tx power @ 24 dBm			
5G SA (1 Tx)	5G NR LB @ 23 dBm	n5	TBD	mA
	5G NR MB @ 23 dBm	n1	TBD	mA
	5G NR HB @ 23 dBm	n7	TBD	mA
	5G NR UHB @ 26 dBm	n78	TBD	mA
5G SA (2 Tx)	5G NR UL 2 × 2 MIMO @ 26 dBm	n78	TBD	mA
LTE + 5G EN-DC	LTE DL, 256QAM	DC_3A_n78A	TBD	mA
	LTE UL QPSK			
	NR DL, 256QAM			

	NR UL QPSK
	LTE Tx Power @ 23 dBm
	NR Tx Power @ 23 dBm

NOTE

1. The power consumption test is performed with EVB at room temperature without any thermal dissipation measure.
2. The power consumption above is for reference only, please contact Quectel Technical Support for detailed power consumption test report of the module.

6.4. Digital I/O Characteristic

Table 40: Logic Levels of 1.8 V Digital I/O

Parameter	Description	Min.	Max.	Unit
VDDIO_1V8	Supply voltage	1.7	1.94	V
V_{IH}	High-level input voltage	0.65 × VDDIO_1V8	VDDIO_1V8 + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.35 × VDDIO_1V8	V
V_{OH}	High-level output voltage	VDDIO_1V8 - 0.45	-	V
V_{OL}	Low-level output voltage	-	0.45	V

Table 41: Logic Levels of 3.3 V Digital I/O

Parameter	Description	Min.	Max.	Unit
3.3 V	Supply voltage	3.135	3.465	V
V_{IH}	High-level input voltage	2.0	3.6	V
V_{IL}	Low-level input voltage	-0.5	0.8	V

Table 42: (U)SIM High/Low-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	0.7 × USIM_VDD	USIM_VDD + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.2 × USIM_VDD	V
V_{OH}	High-level output voltage	0.8 × USIM_VDD	-	V
V_{OL}	Low-level output voltage	-	0.4	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 43: Electrostatic Discharge Characteristics (Temperature: 25–30 ºC, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VCC, GND	±5	±10	kV
Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

Table 44: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Normal Operating Temperature [19]	-30	+25	+75	ºC
Extended Operating Temperature [20]	-40	-	+85	ºC
Storage Temperature	-40	-	+90	ºC

6.7. Thermal Dissipation

The module offers the best performance when all internal IC chips are working within their operating temperatures. When the IC chip reaches or exceeds the maximum junction temperature, the module may still work but the performance and function (such as RF output power, data rate, etc.) will be affected to a certain extent. Therefore, the thermal design should be maximally optimized to ensure all internal IC chips always work within the recommended operating temperature range.

The following principles for thermal consideration are provided for reference:

- Keep the module away from heat sources on your PCB, especially high-power components such as processor, power amplifier, and power supply.
- Maintain the integrity of the PCB copper layer and drill as many thermal vias as possible.
- Expose the copper in the PCB area where module is mounted.
- Apply a soft thermal pad with appropriate thickness and high thermal conductivity between the module and the PCB to conduct heat.
- Follow the principles below when the heatsink is necessary:
  - Do not place large size components in the area where the module is mounted on your PCB to reserve enough place for heatsink installation.
  - Attach the heatsink to the shielding cover of the module; In general, the base plate area of the heatsink should be larger than the module area to cover the module completely.

[19] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heat sinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

[20] To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heat sinks, heat pipes, vapor chambers. Within this range, the module retains the ability to establish and maintain functions such as voice*, SMS, data transmission and emergency call*, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as Pout, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

- Choose the heatsink with adequate fins to dissipate heat.
- Choose a TIM (Thermal Interface Material) with high thermal conductivity, good softness and good wettability and place it between the heatsink and the module.
- Fasten the heatsink with four screws to ensure that it is in close contact with the module to prevent the heatsink from falling off during the drop, vibration test, or transportation.

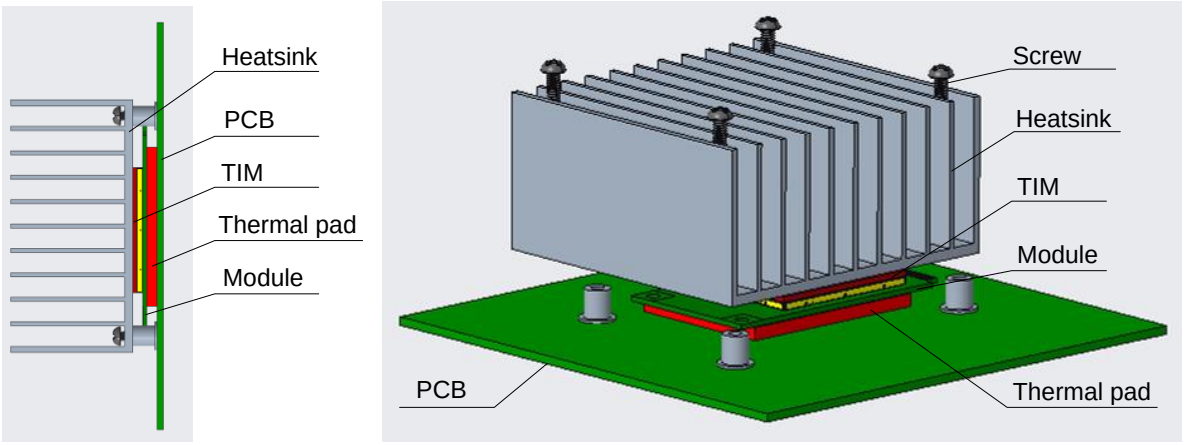


Figure 36: Placement and Fixing of the Heatsink

7 Storage and Packaging

7.1. Storage Conditions

The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life: 12 months in Recommended Storage Condition.

NOTE

Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

7.2. Notification

Please follow the principles below in module application.

7.2.1. Coating

If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.

7.2.2. Cleaning

Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.

7.2.3. Installing

The module needs to be fixed firmly to avoid poor contact caused by shaking. When installing the module, it is recommended to be mounted on the socket with a screw as shown below.

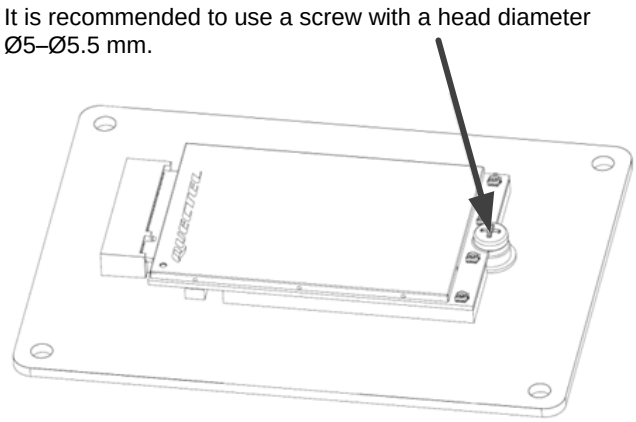


Figure 37: Installation Schematic

7.3. Packaging

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts blister tray packaging and details are as follow.

7.3.1. Blister Tray

Dimension details are as follow:

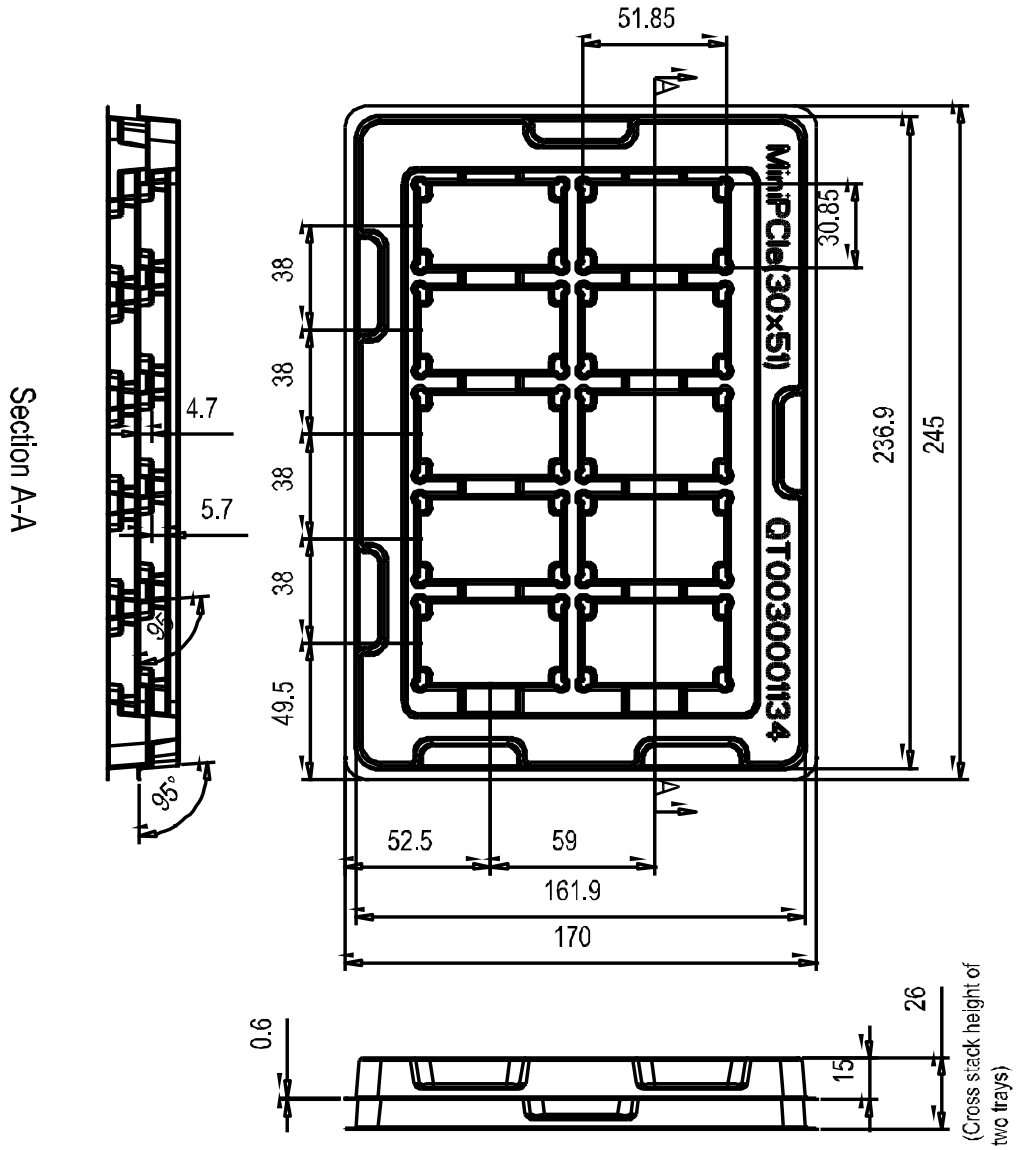
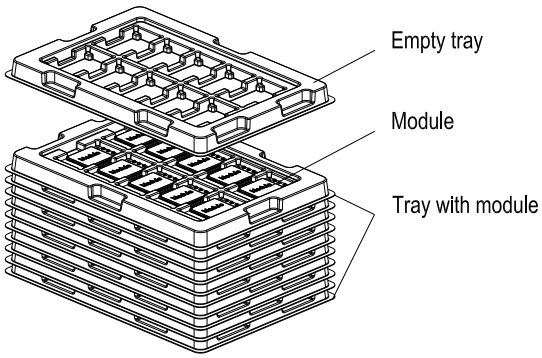
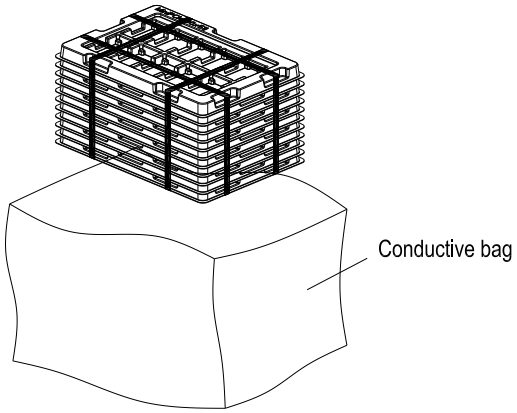


Figure 38: Blister Tray Dimension Drawing

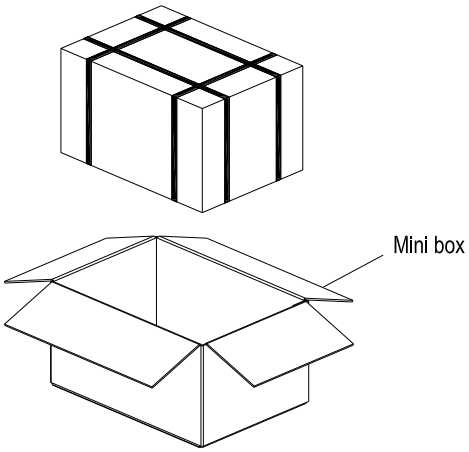
7.3.2. Packaging Process



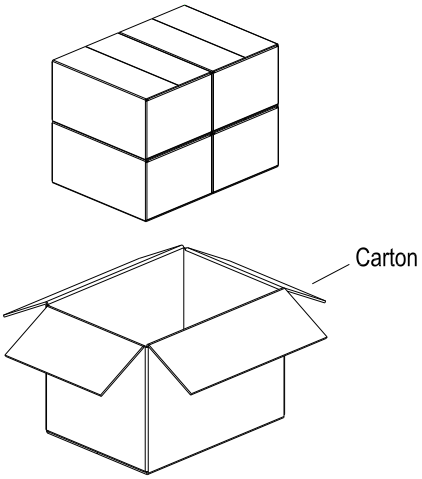
Pack 10 modules in each blister tray. Stack 10 blister trays with modules together, and put 1 empty blister tray on the top.



Pack 11 blister trays together and then put these blister trays into a conductive bag, seal and pack the conductive bag.



Put seal-packed blister trays into a mini box. One mini box contains 100 modules.



Put 4 mini boxes into 1 carton and then seal it. One carton can pack 400 modules.

Figure 39: Packaging Process

8 Appendix A References

Table 45: Related Documents

Document Name
[1] Quectel_RM551E-GL_Reference_Design
[2] Quectel_RM551E-GL_CA&EN-DC_Features
[3] Quectel_5G-M2_EVB_User_Guide
[4] Quectel_RG520N&RG525F&RG5x0F&RM5x0N_Series_AT_Commands_Manual
[5] Quectel_RG520N&RG525F&RG5x0F&RM5x0N_Series_GNSS_Application_Note
[6] Quectel_RG520N&RG525F&RG5x0F&RM5x0N_Series_RF_Application_Note
[7] Quectel_5G-mmWave_EVB_User_Guide

Table 46: Reference Standards

Abbreviation	Description
PCIe M.2 Specification	*PCI Express M.2 Specification Revision 4.0*
PCIe 4.0 Specification	*PCI Express Base Specification Revision 4.0*
USB 3.1 Specification	*Universal Serial Bus 3.1 Specification*
-	*ISO/IEC 7816-3*
-	*MIPI Alliance Specification for RF Front-End Control Interface version 2.0*
-	*3GPP TS 27.007 and 3GPP TS 27.005*

Table 47: Terms and Abbreviations

Abbreviation	Description
APT	Average Power Tracking
BIOS	Basic Input Output System
bps	Bit Per Second
CHAP	Challenge-Handshake Authentication Protocol
COEX	Coexistence
DC-DC	Direct Current to Direct Current
DFOTA	Delta Firmware Upgrade Over-The-Air
DC-HSDPA	Dual-carrier High Speed Downlink Packet Access
DL	Downlink
DPR	Dynamic Power Reduction
DRX	Discontinuous Reception (***Chapter 3.1.1***) Diversity Reception (***Chapter 5***)
EN-DC	E-UTRA New Radio Dual Connectivity
EP	End Point
ESD	Electrostatic Discharge
E-UTRA	Evolved Universal Terrestrial Radio Access
FDD	Frequency Division Duplexing
FOTA	Firmware Over-The-Air
GLONASS	Global Navigation Satellite System (Russia)
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HB	High Band
HPUE	High Power User Equipment
HSDPA	High Speed Downlink Packet Access

HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
IC	Integrated Circuit
kbps	Kilo Bits Per Second
LAA	License Assisted Access
LED	Light Emitting Diode
LTE	Long Term Evolution
MB	Middle Band
Mbps	Mega Bits Per Second
ME	Mobile Equipment
MIMO	Multiple-Input Multiple-Output
MLCC	Multilayer Ceramic Chip Capacitor
MO	Mobile Originated
MSB	Most Significant Bit
MT	Mobile Terminated
NR	New Radio
PAP	Password Authentication Protocol
PC	Power Class
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
PRX	Primary Receive
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RC	Root Complex

RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
RFFE	RF Front-End
Rx	Receive
SAR	Specific Absorption Rate
SCS	Sub-Carrier Spacing
SIMO	Single Input Multiple Output
SMS	Short Message Service
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
TTFF	Time to First Fix
Tx	Transmit
UART	Universal Asynchronous Receiver & Transmitter
UDP	User Datagram Protocol
UHB	Ultra High Band
UL	Uplink
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
V_{IH}	High-level Input Voltage
V_{IL}	Low-level Input Voltage
V_{OH}	High-level Output Voltage
V_{OL}	Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
WWAN	Wireless Wide Area Network

9 Appendix B Operating Frequency

Table 48: Operating Frequencies (5G)

5G	Duplex Mode	Uplink Operating Band	Downlink Operating Band	Unit
n1	FDD	1920–1980	2110–2170	MHz
n2	FDD	1850–1910	1930–1990	MHz
n3	FDD	1710–1785	1805–1880	MHz
n5	FDD	824–849	869–894	MHz
n7	FDD	2500–2570	2620–2690	MHz
n8	FDD	880–915	925–960	MHz
n12	FDD	699–716	729–746	MHz
n13	FDD	777–787	746–756	MHz
n14	FDD	788–798	758–768	MHz
n18	FDD	815–830	860–875	MHz
n20	FDD	832–862	791–821	MHz
n24	FDD	1626.5–1660.5	1525–1559	MHz
n25	FDD	1850–1915	1930–1995	MHz
n26	FDD	814–849	859–894	MHz
n28	FDD	703–748	758–803	MHz
n29	SDL	-	717–728	MHz
n30	FDD	2305–2315	2350–2360	MHz
n34	TDD	2010–2025	2010–2025	MHz
n38	TDD	2570–2620	2570–2620	MHz

n39	TDD	1880–1920	1880–1920	MHz
n40	TDD	2300–2400	2300–2400	MHz
n41	TDD	2496–2690	2496–2690	MHz
n46	TDD	5150–5925	5150–5925	MHz
n47	TDD	5855–5925	5855–5925	MHz
n48	TDD	3550–3700	3550–3700	MHz
n50	TDD	1432–1517	1432–1517	MHz
n51	TDD	1427–1432	1427–1432	MHz
n53	TDD	2483.5–2495	2483.5–2495	MHz
n65	FDD	1920–2010	2110–2200	MHz
n66	FDD	1710–1780	2110–2200	MHz
n67	SDL	-	738–758	MHz
n70	FDD	1695–1710	1995–2020	MHz
n71	FDD	663–698	617–652	MHz
n74	FDD	1427–1470	1475–1518	MHz
n75	SDL	-	1432–1517	MHz
n76	SDL	-	1427–1432	MHz
n77	TDD	3300–4200	3300–4200	MHz
n78	TDD	3300–3800	3300–3800	MHz
n79	TDD	4400–5000	4400–5000	MHz
n80	SUL	1710–1785	-	MHz
n81	SUL	880–915	-	MHz
n82	SUL	832–862	-	MHz
n83	SUL	703–748	-	MHz
n84	SUL	1920–1980	-	MHz
n85	FDD	698–716	728–746	MHz

n86	SUL	1710–1780	-	MHz
n89	SUL	824–849	-	MHz
n90	TDD	2496–2690	2496–2690	MHz
n91	FDD	832–862	1427–1432	MHz
n92	FDD	832–862	1432–1517	MHz
n93	FDD	880–915	1427–1432	MHz
n94	FDD	880–915	1432–1517	MHz
n95	SUL	2010–2025	-	MHz
n96	TDD	5925–7125	5925–7125	MHz
n97	SUL	2300–2400	-	MHz
n98	SUL	1880–1920	-	MHz
n99	SUL	1626.5–1660.5	-	MHz

Table 49: Operating Frequencies (2G + 3G + 4G)

2G	3G	4G	Duplex Mode	Uplink	Downlink	Unit
-	B1	B1	FDD	1920–1980	2110–2170	MHz
PCS1900	B2/BC1	B2	FDD	1850–1910	1930–1990	MHz
DCS1800	B3	B3	FDD	1710–1785	1805–1880	MHz
-	B4	B4	FDD	1710–1755	2110–2155	MHz
GSM850	B5/BC0	B5	FDD	824–849	869–894	MHz
-	B6	-	FDD	830–840	875–885	MHz
-	B7	B7	FDD	2500–2570	2620–2690	MHz
EGSM900	B8	B8	FDD	880–915	925–960	MHz
-	B9	B9	FDD	1749.9–1784.9	1844.9–1879.9	MHz
-	B10	B10	FDD	1710–1770	2110–2170	MHz
-	B11	B11	FDD	1427.9–1447.9	1475.9–1495.9	MHz

-	B12	B12	FDD	699–716	729–746	MHz
-	B13	B13	FDD	777–787	746–756	MHz
-	B14	B14	FDD	788–798	758–768	MHz
-	-	B17	FDD	704–716	734–746	MHz
-	-	B18	FDD	815–830	860–875	MHz
-	B19	B19	FDD	830–845	875–890	MHz
-	B20	B20	FDD	832–862	791–821	MHz
-	B21	B21	FDD	1447.9–1462.9	1495.9–1510.9	MHz
-	B22	B22	FDD	3410–3490	3510–3590	MHz
-	-	B24	FDD	1626.5–1660.5	1525–1559	MHz
-	B25	B25	FDD	1850–1915	1930–1995	MHz
-	B26	B26	FDD	814–849	859–894	MHz
-	-	B27	FDD	807–824	852–869	MHz
-	-	B28	FDD	703–748	758–803	MHz
-	-	B29	FDD [21]	-	717–728	MHz
-	-	B30	FDD	2305–2315	2350–2360	MHz
-	-	B31	FDD	452.5–457.5	462.5–467.5	MHz
-	-	B32	FDD [21]	-	1452–1496	MHz
-	B33	B33	TDD	1900–1920	1900–1920	MHz
-	B34	B34	TDD	2010–2025	2010–2025	MHz
-	B35	B35	TDD	1850–1910	1850–1910	MHz
-	B36	B36	TDD	1930–1990	1930–1990	MHz
	B37	B37	TDD	1910–1930	1910–1930	MHz
-	B38	B38	TDD	2570–2620	2570–2620	MHz
-	B39	B39	TDD	1880–1920	1880–1920	MHz

[21] Restricted to E-UTRA operation when carrier aggregation is configured. The downlink operating band is paired with the uplink operating band (external) of the carrier aggregation configuration that is supporting the configured Pcell.

-	B40	B40	TDD	2300–2400	2300–2400	MHz
-	-	B41	TDD	2496–2690	2496–2690	MHz
-	-	B42	TDD	3400–3600	3400–3600	MHz
-	-	B43	TDD	3600–3800	3600–3800	MHz
-	-	B44	TDD	703–803	703–803	MHz
-	-	B45	TDD	1447–1467	1447–1467	MHz
-	-	B46	TDD	5150–5925	5150–5925	MHz
-	-	B47	TDD	5855–5925	5855–5925	MHz
-	-	B48	TDD	3550–3700	3550–3700	MHz
-	-	B50	TDD	1432–1517	1432–1517	MHz
-	-	B51	TDD	1427–1432	1427–1432	MHz
-	-	B52	TDD	3300–3400	3300–3400	MHz
-	-	B65	FDD	1920–2010	2110–2200	MHz
-	-	B66	FDD	1710–1780	2110–2200 [22]	MHz
-	-	B67	FDD [21]	-	738–758	MHz
-	-	B68	FDD	698–728	753–783	MHz
-	-	B69	FDD [21]	-	2570–2620	MHz
-	-	B70	FDD [23]	1695–1710	1995–2020	MHz
-	-	B71	FDD	663–698	617–652	MHz
-	-	B72	FDD	451–456	461–466	MHz
-	-	B73	FDD	450–455	460–465	MHz
-	-	B74	FDD	1427–1470	1475–1518	MHz
-	-	B75	FDD [21]	-	1432–1517	MHz

[22] The range 2180–2200 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured.
[23] The range 2010–2020 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured and TX-RX separation is 300 MHz. The range 2005–2020 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured and TX-RX separation is 295 MHz.

-	-	B76	FDD [21]	-	1427–1432	MHz
-	-	B85	FDD	698–716	728–746	MHz
-	-	B87	FDD	410–415	420–425	MHz
-	-	B88	FDD	412–417	422–427	MHz