# RM50xQ Series
# Reference Design for Laptop

**5G Module Series**

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# About the Document

## Revision History

| Version | Date | Author | Description |
|---------|------|--------|-------------|
| 1.0 | 2020-09-15 | Oscar LIU/ Jumping HE | Initial |
| 1.1 | 2021-04-12 | Norton ZHANG | 1. Updated document's application scope form RM500Q series to RM50xQ series.<br>2. Updated VCC reference circuit.<br>3. Updated the pin name of pin 67 from RESET_N to RESET#; pins 2, 4, 70, 72, and 74 from VCC_MODULE to VCC; pin 6 from FULL_CARD_PWR_OFF# to FULL_CARD_POWER_OFF#. |
| 1.2 | 2023-12-22 | Norton ZHANG | Added a note on avoiding abnormal RF functions caused by current sink on the module's pins (Sheet 1). |

# Contents

# 1 Reference Design

## 1.1. Introduction

This document provides the RM50xQ series reference design for laptops, including that for power supply, connection between laptop and RM50xQ series, and (U)SIM interfaces.

The document is applicable to the following modules:

- RM500Q series
- RM502Q series
- RM505Q-AE

## 1.2. Schematics

The schematics illustrated in the following pages are provided for reference only.

# Block Diagram



Compatible Design

VCC_5V → Buck → 3.3 V → 0R

VCC_3V3 → MOS/Load Switch → 3.3 V → 0R

EN

Laptop
- PCIe × 1 Interface
- USB 3.1 Interface
- GPIO Control

VCC

M.2 Socket

RM50xQ Series

(U)SIM1   (U)SIM2
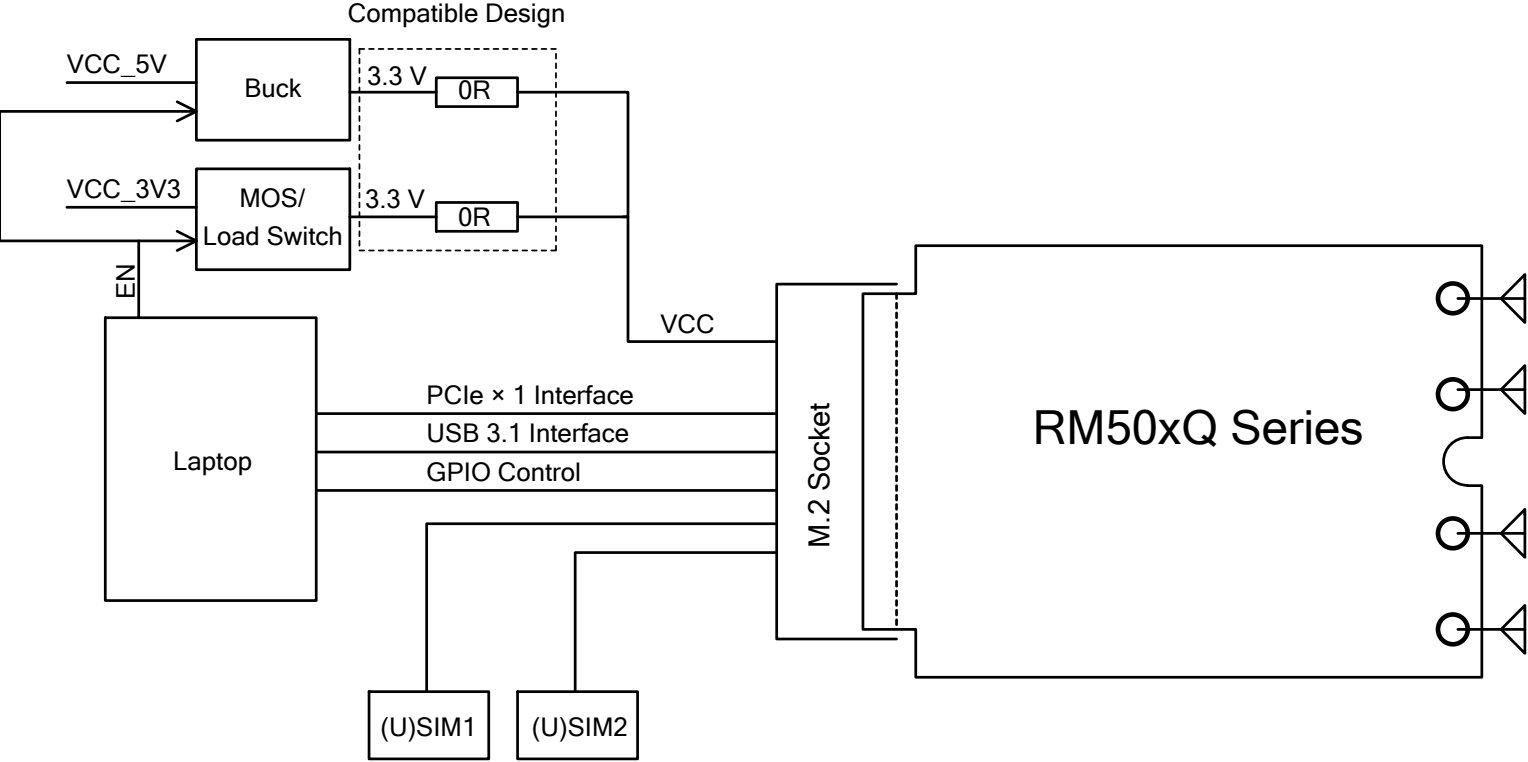
Note:

1. The location of anntena connectors is for reference only. For more details about antenna connectors, see *Quectel_RM50xQ_Series_Hardware_Design*.
2. Before the module turns on, ensure the pins DPR and USIM_DET are not pulled high to avoid current sink damaging the module. For more details, contact Quectel Technical Support.

# Power Supply Design

$Lmin = (Vin - Vout) \times Vout / (0.4 \times Iout(max.) \times Fsw \times Vin) = (5.0\ V - 3.3\ V) \times 3.3\ V / (0.4 \times 3.0\ A \times 1.0\ MHz \times 5.0\ V) = 0.935\ \mu H$

U101
TPS54319RTER

1.5 µH +/-20 % 0.065 Ω 4.5 A

VCC_5V

C101 220µF
C102 220µF
C103 100nF
C104 33pF

R101 205K
R102 80.6K

[2] VREF

PWR_EN [2,4]

Q101 DTC043ZEB

R103 10K
R104 182K
C113 10nF
C111 NM_0.5pF
C112 10nF

**U101 pins:**
16 VIN
1 VIN
2 VIN
15 EN
6 VSNS
7 COMP
8 RT/CLK
9 SS
10 PH
11 PH
12 PH
13 BOOT
14 PWRGD
3 GND
4 GND
5 AGND
17 PWPD

C106 100nF

L101

C107 100µF
C108 100µF
C109 100nF
C110 33pF
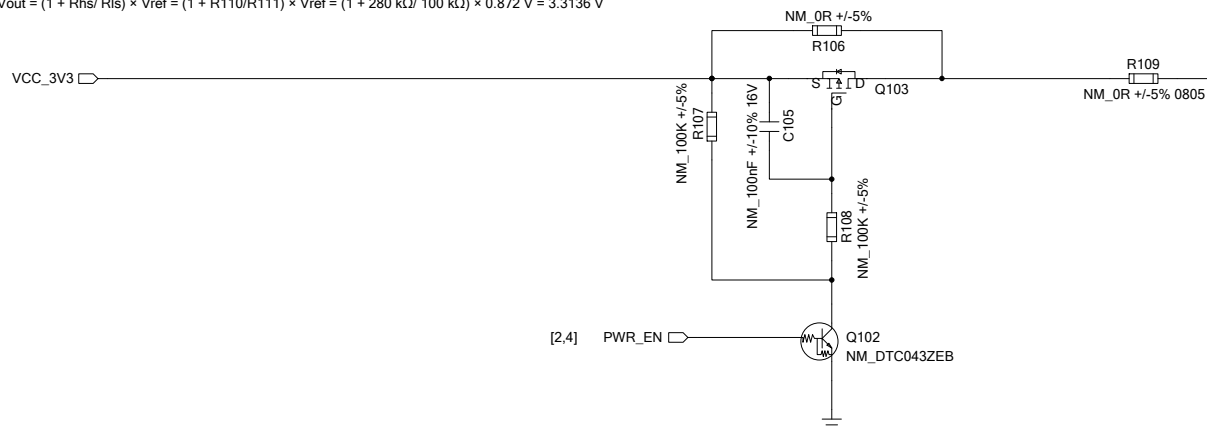
R105 0R +/-5% 0805

VCC_MODULE [3]

R110 280K
VREF [2]
R111 100K

**Input UVLO**
Ruvlo1 = R101 = 205 kΩ,  Ruvlo2 = R102 = 80.6 kΩ
Vstart = 4.006 V, Vstop = 3.309 V
Rt = R104 = 182 kΩ, Fsw = 1.0 MHz
$Vout = (1 + Rhs/ Rls) \times Vref = (1 + R110/R111) \times Vref = (1 + 280\ k\Omega/ 100\ k\Omega) \times 0.872\ V = 3.3136\ V$

NM_0R +/-5%
R106

VCC_3V3

R107 NM_100K +/-5%
C105 NM_100nF +/-10% 16V
Q103
R108 NM_100K +/-5%
R109 NM_0R +/-5% 0805

PWR_EN [2,4]

Q102 NM_DTC043ZEB

**Notes:**

1. The power supply must be able to provide sufficient current up to 3 A or higher.
2. A compatible design is recommended for VCC power supply.

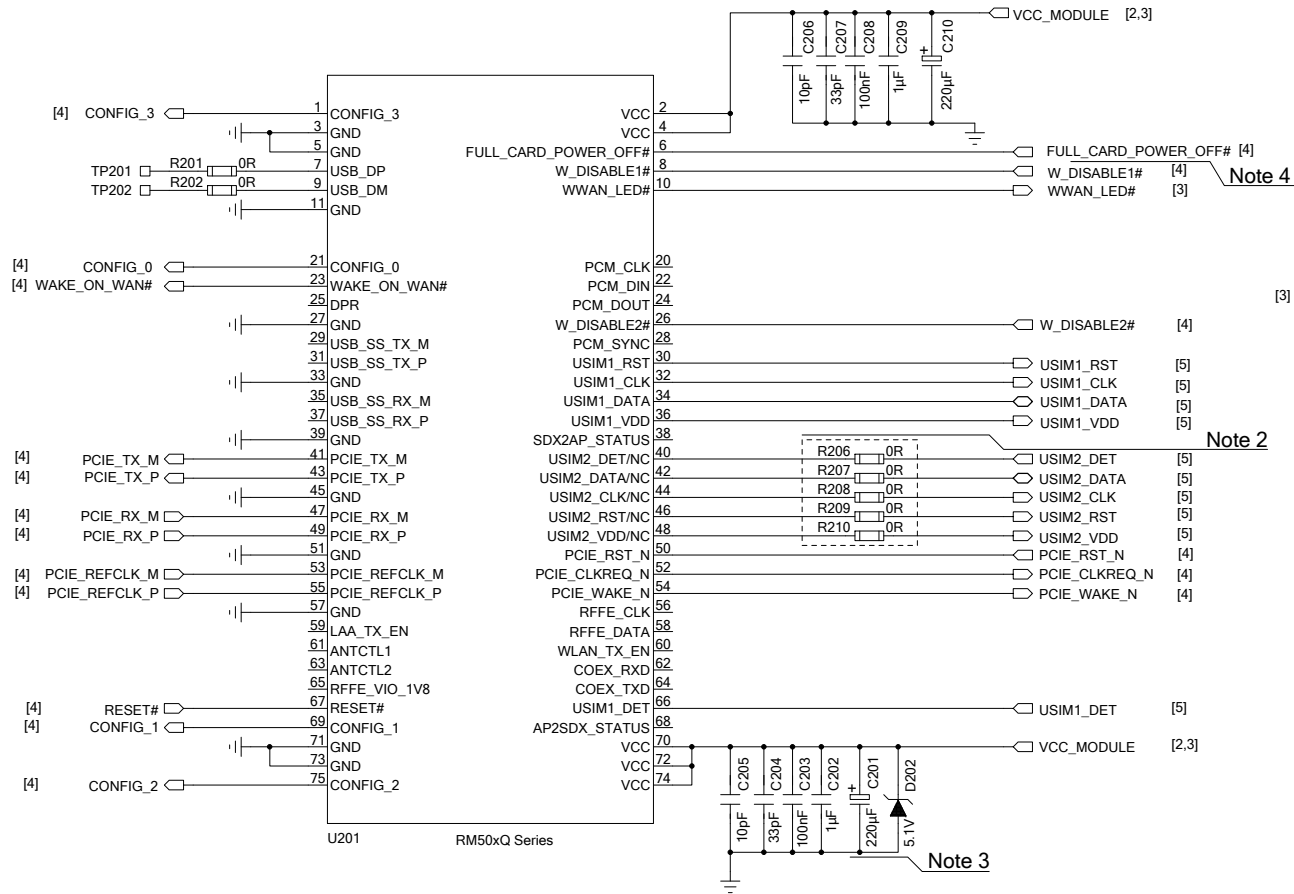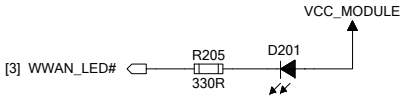# Connectivity Between Laptop and RM50xQ Series (Part 1)

| FULL_CARD_POWER_OFF# | Module |
|---|---|
| H | Turn On |
| L | Turn Off |

VCC_MODULE [2,3]

C206 10pF | C207 33pF | C208 100nF | C209 1µF | C210 220µF

FULL_CARD_POWER_OFF# [4]
W_DISABLE1# [4]
WWAN_LED# [3]

Note 4

VCC_MODULE

[3] WWAN_LED#    R205 330R    D201

**U201 — RM50xQ Series**

| Pin | Signal |
|---|---|
| 1 | CONFIG_3 |
| 3 | GND |
| 5 | GND |
| 7 | USB_DP |
| 9 | USB_DM |
| 11 | GND |
| 21 | CONFIG_0 |
| 23 | WAKE_ON_WAN# |
| 25 | DPR |
| 27 | GND |
| 29 | USB_SS_TX_M |
| 31 | USB_SS_TX_P |
| 33 | GND |
| 35 | USB_SS_RX_M |
| 37 | USB_SS_RX_P |
| 39 | GND |
| 41 | PCIE_TX_M |
| 43 | PCIE_TX_P |
| 45 | GND |
| 47 | PCIE_RX_M |
| 49 | PCIE_RX_P |
| 51 | GND |
| 53 | PCIE_REFCLK_M |
| 55 | PCIE_REFCLK_P |
| 57 | GND |
| 59 | LAA_TX_EN |
| 61 | ANTCTL1 |
| 63 | ANTCTL2 |
| 65 | RFFE_VIO_1V8 |
| 67 | RESET# |
| 69 | CONFIG_1 |
| 71 | GND |
| 73 | GND |
| 75 | CONFIG_2 |

Left-side nets:
- [4] CONFIG_3
- TP201 R201 0R USB_DP
- TP202 R202 0R USB_DM
- [4] CONFIG_0
- [4] WAKE_ON_WAN#
- [4] PCIE_TX_M
- [4] PCIE_TX_P
- [4] PCIE_RX_M
- [4] PCIE_RX_P
- [4] PCIE_REFCLK_M
- [4] PCIE_REFCLK_P
- [4] RESET#
- [4] CONFIG_1
- [4] CONFIG_2

Right-side pins:

| Pin | Signal |
|---|---|
| 2 | VCC |
| 4 | VCC |
| 6 | FULL_CARD_POWER_OFF# |
| 8 | W_DISABLE1# |
| 10 | WWAN_LED# |
| 20 | PCM_CLK |
| 22 | PCM_DIN |
| 24 | PCM_DOUT |
| 26 | W_DISABLE2# |
| 28 | PCM_SYNC |
| 30 | USIM1_RST |
| 32 | USIM1_CLK |
| 34 | USIM1_DATA |
| 36 | USIM1_VDD |
| 38 | SDX2AP_STATUS |
| 40 | USIM2_DET/NC |
| 42 | USIM2_DATA/NC |
| 44 | USIM2_CLK/NC |
| 46 | USIM2_RST/NC |
| 48 | USIM2_VDD/NC |
| 50 | PCIE_RST_N |
| 52 | PCIE_CLKREQ_N |
| 54 | PCIE_WAKE_N |
| 56 | RFFE_CLK |
| 58 | RFFE_DATA |
| 60 | WLAN_TX_EN |
| 62 | COEX_RXD |
| 64 | COEX_TXD |
| 66 | USIM1_DET |
| 68 | AP2SDX_STATUS |
| 70 | VCC |
| 72 | VCC |
| 74 | VCC |

Right-side nets:
- W_DISABLE2# [4]
- USIM1_RST [5]
- USIM1_CLK [5]
- USIM1_DATA [5]
- USIM1_VDD [5]   Note 2
- USIM2_DET [5]
- USIM2_DATA [5]
- USIM2_CLK [5]
- USIM2_RST [5]
- USIM2_VDD [5]
- PCIE_RST_N [4]
- PCIE_CLKREQ_N [4]
- PCIE_WAKE_N [4]
- USIM1_DET [5]
- VCC_MODULE [2,3]

R206 0R / R207 0R / R208 0R / R209 0R / R210 0R

C205 10pF | C204 33pF | C203 100nF | C202 1µF | C201 220µF | D202 5.1V

Note 3

## RM50xQ Series

| Module | Pin 40, 42, 44, 46, 48 |
|---|---|
| RM500Q-GL | (U)SIM2 Interface |
| RM502Q-GL | (U)SIM2 Interface |
| RM500Q-AE | NC |
| RM502Q-AE | NC |
| RM505Q-AE | (U)SIM2 Interface |
| RM500Q-CN | (U)SIM2 Interface |

## Notes:

1. It is recommended to reserve test points for the firmware upgrade over USB 2.0 interface and to minimize the stub length of USB test signals.

2. R206 to R210 should be placed close to the M.2 socket. If the module has a built-in eSIM, R206 to R210 should not be mounted.
   RM500Q-AE & RM502Q-AE do not suppport (U)SIM2 interface.

3. It is recommended to use a zener diode D202 with a reverse zener voltage of 5.1 V and it should be placed close to the module pin.

4. Use a laptop GPIO to control FULL_CARD_POWER_OFF# of the module.

# Connectivity Between Laptop and RM50xQ Series (Part 2)

VCC_IO_LAPTOP

R301 10k
R302 10k
R303 NM_10k

U301

| Signal | | |
|---|---|---|
| PCIE_WAKE | PCIE_WAKE_N | [3] |
| PCIE_CLKREQ | PCIE_CLKREQ_N | [3] |
| PCIE_RESET | PCIE_RST_N | [3] |

R315 10k

PCIE0_TXP — C301 220nF — PCIE_RX_P [3]
PCIE0_TXN — C302 220nF — PCIE_RX_M [3]

PCIE0_RXP — PCIE_TX_P [3]
PCIE0_RXN — PCIE_TX_M [3]

PCIE0_CLK_P — R313 0R — PCIE_REFCLK_P [3]
PCIE0_CLK_N — R314 0R — PCIE_REFCLK_M [3]

[4] TURN_ON/OFF — R311 0R — FULL_CARD_POWER_OFF# [3]

VCC_IO_LAPTOP

R304 100k
R305 100k
R306 100k

R312 NM_0R — RESET# [3]

GPIO_XX — W_DISABLE1# [3]
GPIO_XX — W_DISABLE2# [3]

[4] RESET — Q302 DTC043ZEB

GPIO_XX — WAKE_ON_WAN# [3]
GPIO_XX

GPIO_XX — RESET [4]
GPIO_XX — TURN_ON/OFF [4]

VCC_IO_LAPTOP

R307 10k
R308 10k
R309 10k
R310 10k

GPIO_XX — PWR_EN [2]

GPIO_XX — CONFIG_0 [3]
GPIO_XX — CONFIG_1 [3]
GPIO_XX — CONFIG_2 [3]
GPIO_XX — CONFIG_3 [3]

Laptop
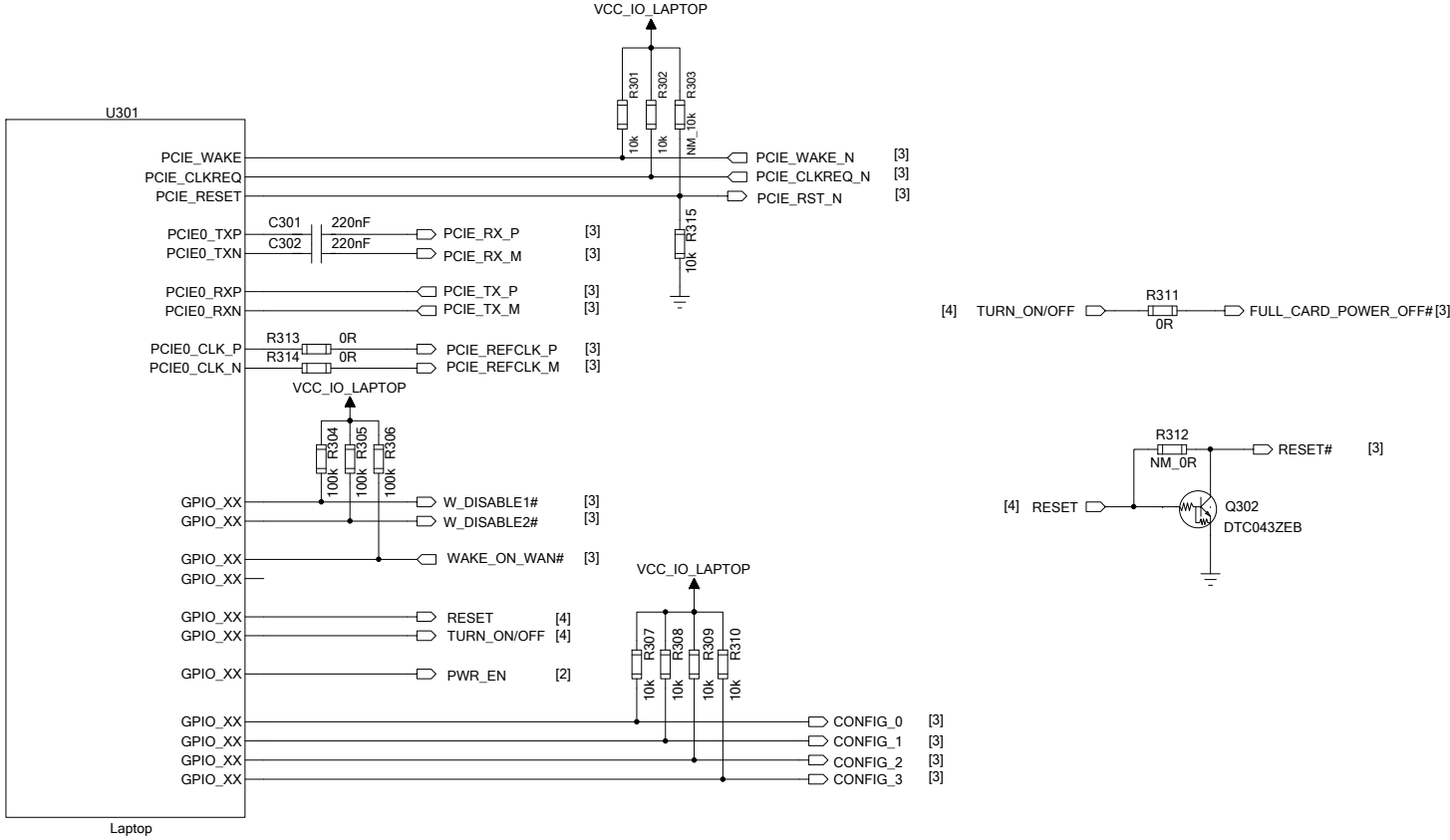
Notes:

1. U301 represents the customer`s host.
2. Keep C301-C302 close to the host.
3. The differential impedance of PCIe signal traces should be controlled to 85 Ω.
4. If a USB connector is used, please keep ESD protection components to the USB conncector as close as possible.

# (U)SIM Interfaces Design

## (U)SIM1



## (U)SIM2
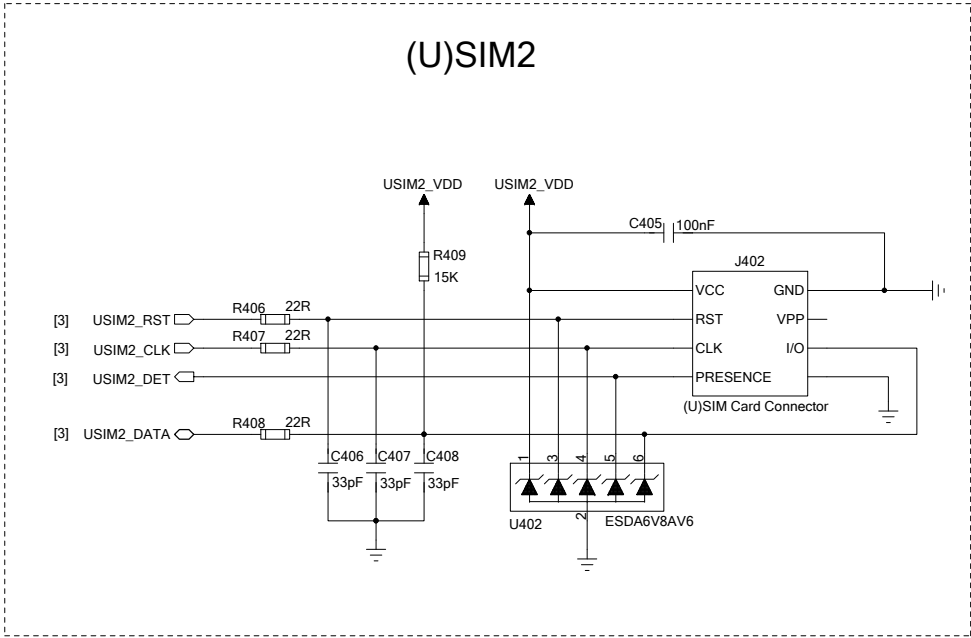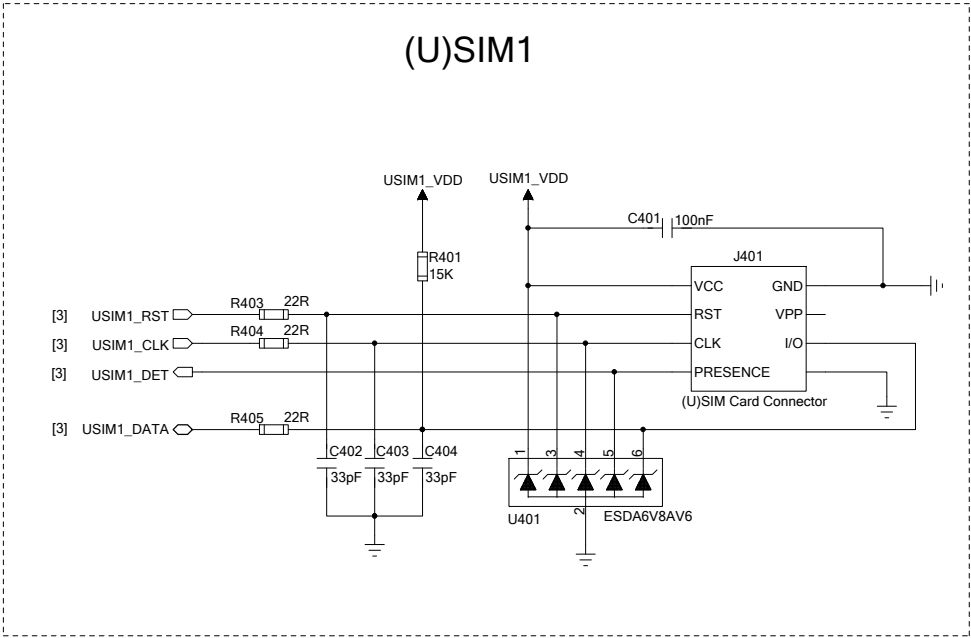


Notes:

1. The decoupling capacitors of (U)SIM signals and (U)SIM related resistors must be placed close to (U)SIM card connectors.
2. RM50xQ series module provides the input pin(s) USIM_DET[1:2] to detect (U)SIM cards.
   1) A normally short-circuited (U)SIM card connector is used in this reference design, and high-logic-level detection is supported. For more details, see corresponding Hardware Design.
   2) This pin is pulled LOW by default, and will be internally pulled up to 1.8 V by software configuration only when (U)SIM hot-plug is enabled by AT+QSIMDET.
3. R403-R408 are applied to suppress the EMI such as spurious transmission.
4. A ESD diode array with a junction capacitance of lower than 10 pF should be placed as close to the (U)SIM card connector as possible for ESD protection.
5. The (U)SIM card connector should be placed near the M.2 socket, because a long trace may lead to wave distortion, which affects the signal quality.