EG12&EG18

Reference Design

LTE-A Module Series

Rev. EG12&EG18_Reference_Design_V1.1

Date: 2019-08-29

Status: Released

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About the Document

History

Revision	Date	Author	Description
1.0	2019-06-20	Oscar LIU/ Jim HAN	Initial
1.1	2019-08-29	Oscar LIU/ Jim HAN	1. Updated the USB_VBUS net 2. Updated the VDD_P2 net and added a note for net connection

Contents

1 Reference Design

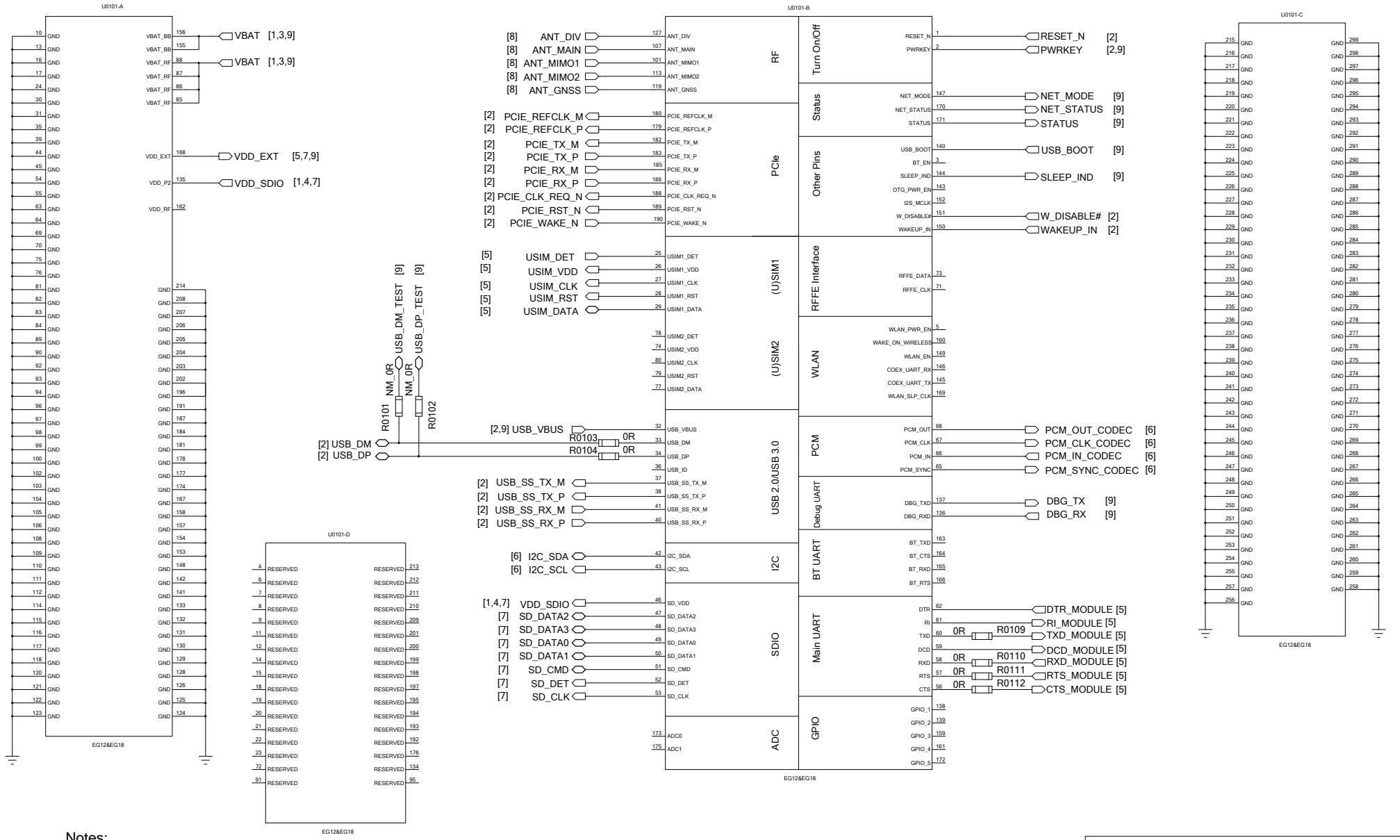
1.1. Introduction

This document provides the reference design for Quectel EG12 and EG18 modules.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Module Interfaces



Notes:

1. ADC pins can not be directly connected to the power supply. The power supply for ADC pins must not exceed 1.875V.
2. It is recommended to reserve the test points for upgrading the firmware over USB interface and minimize the stub length of USB test signals.
3. Keep all RESERVED and unused pins unconnected, and all GND pins connected to the ground network.
4. If an SD card is used, connect VDD_P2 to SD_VDD. If unused, connect VDD_P2 to VDD_EXT.

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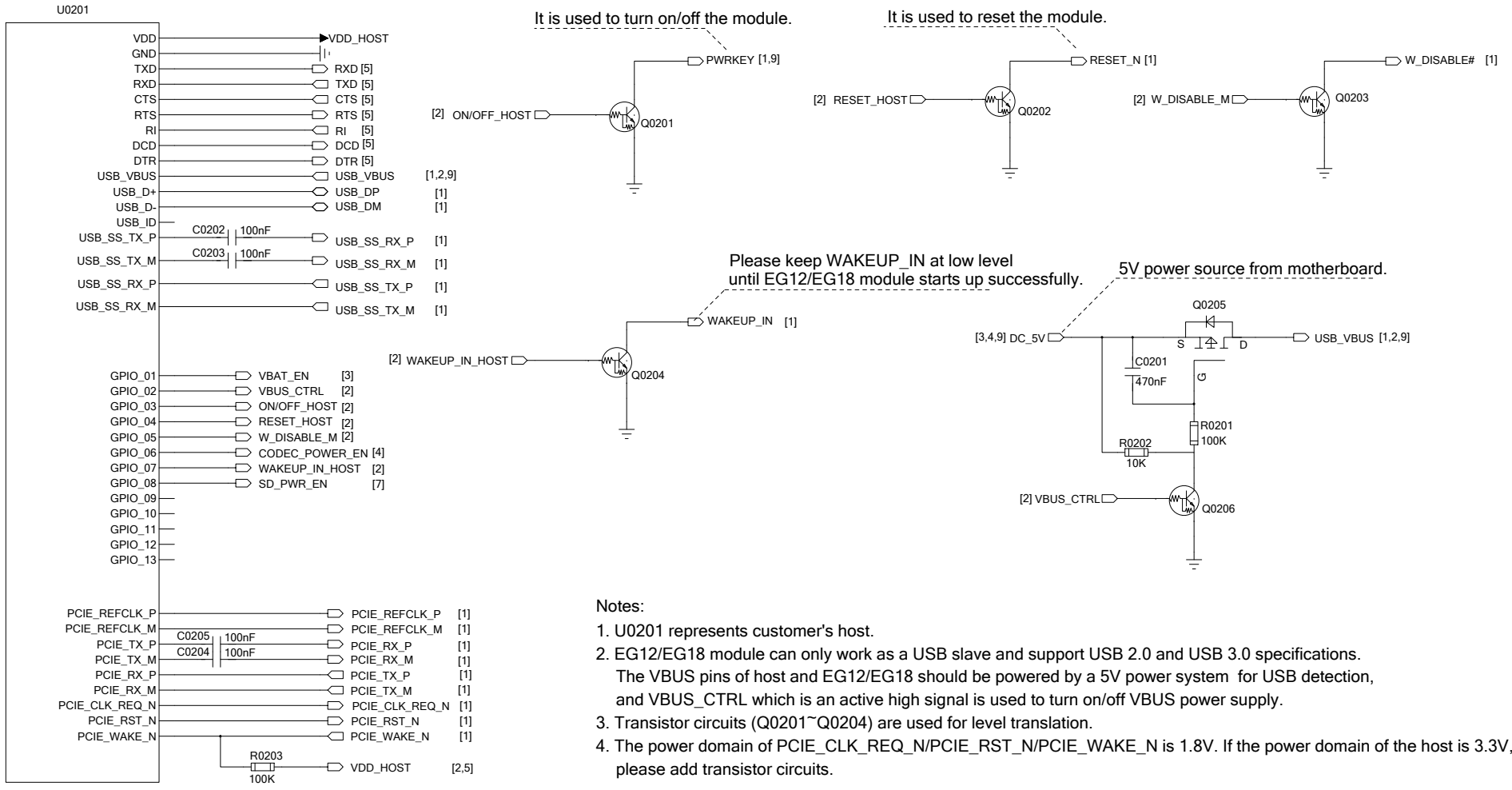
Host Interfaces



Notes:

1. U0201 represents customer's host.
2. EG12/EG18 module can only work as a USB slave and support USB 2.0 and USB 3.0 specifications. The VBUS pins of host and EG12/EG18 should be powered by a 5V power system for USB detection, and VBUS_CTRL which is an active high signal is used to turn on/off VBUS power supply.
3. Transistor circuits (Q0201~Q0204) are used for level translation.
4. The power domain of PCIE_CLK_REQ_N/PCIE_RST_N/PCIE_WAKE_N is 1.8V. If the power domain of the host is 3.3V, please add transistor circuits.

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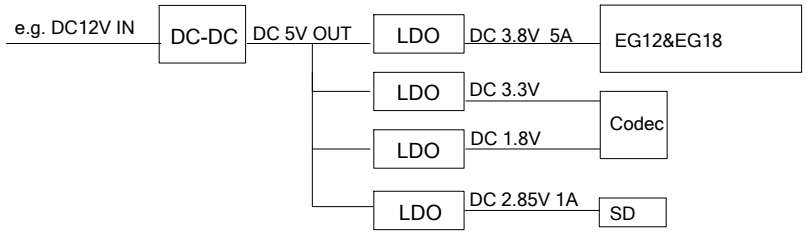
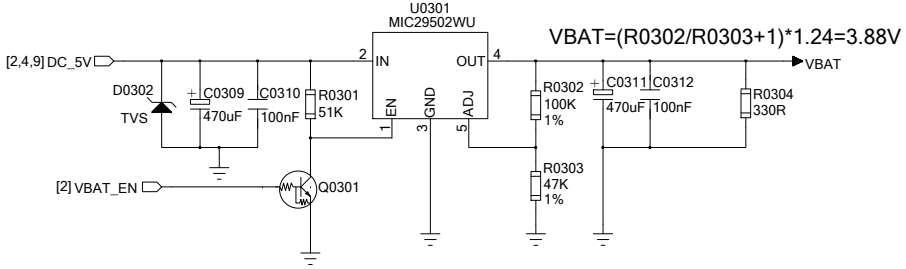
Power Supply (Part 1)

DC-DC Application



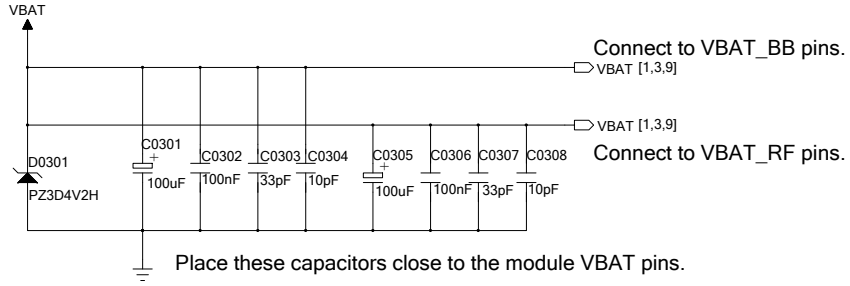
Note:
When the input voltage is above 7V, a DC-DC converter should be used to convert the high input voltage to 5V output, and then the LDOs will generate 3.8V/3.3V/1.8V/2.85V typical voltages.

LDO Application



Note:
The load current of MIC29502WU is recommended to be greater than10mA.

VBAT Design



Notes:
1. The power supply must be able to provide sufficient current up to 2A or more.
2. VBAT should be routed in star mode to VBAT_BB and VBAT_RF pins.
3. The recommended operating voltage of VBAT is 3.3V~4.3V.

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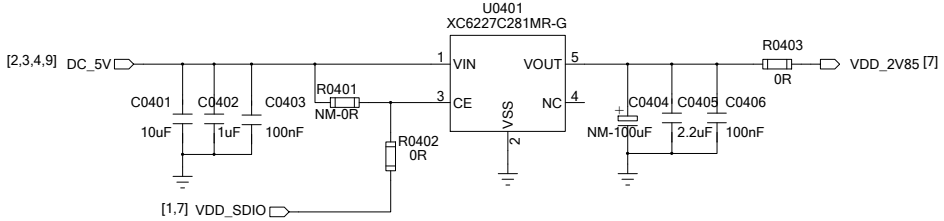
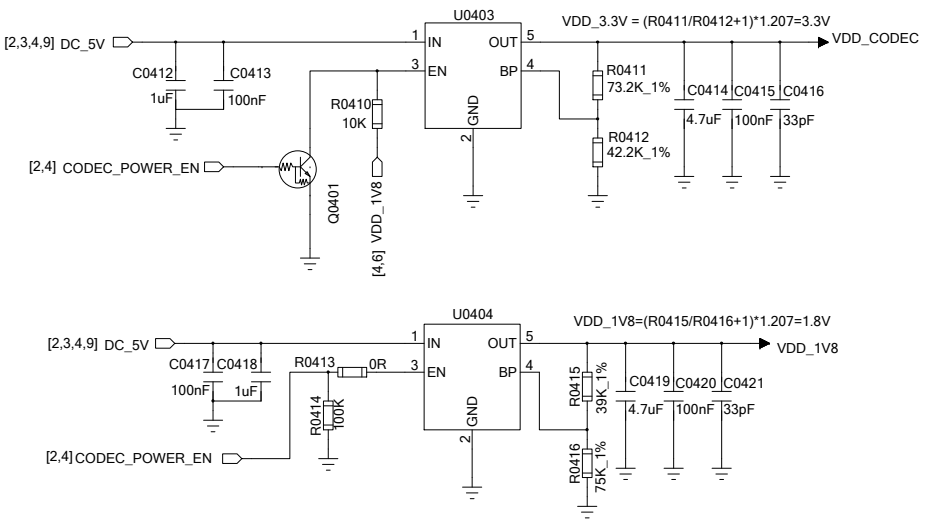
Power Supply (Part 2)

Power Supply for SD Card



Power Supply for PCM Codec



Note:

CODEC_POWER_EN must be at low level in order to ensure the normal output voltage of VDD_3.3V. If VDD_3.3V power supply needs to be switched off, please keep CODEC_POWER_EN at high level.

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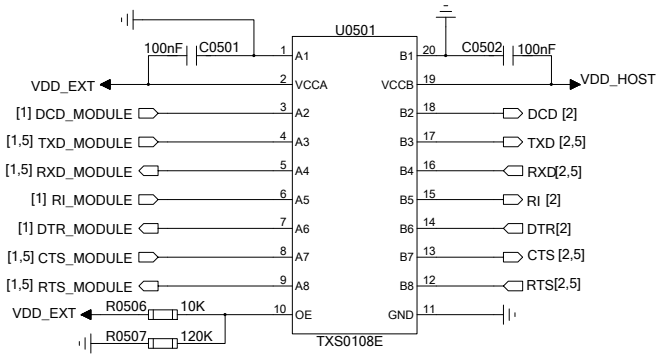
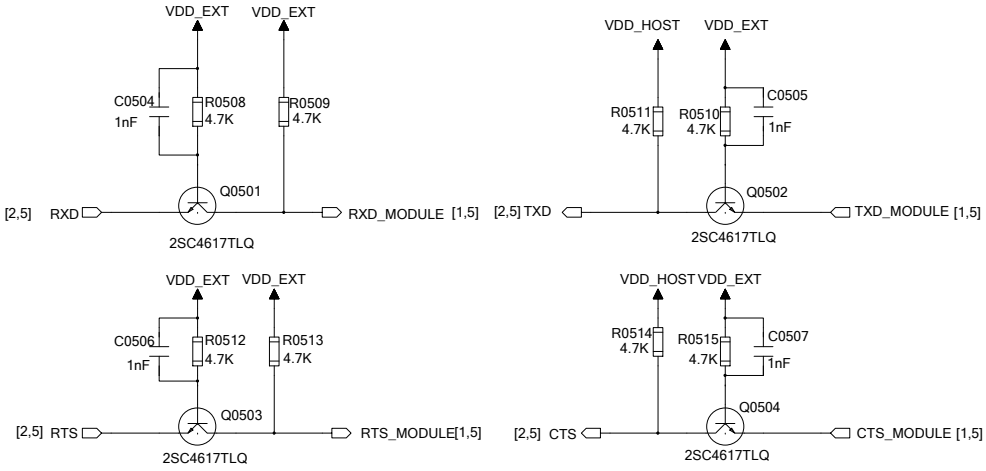
(U)SIM and UART Designs

UART Translation - IC Solution (Recommended)



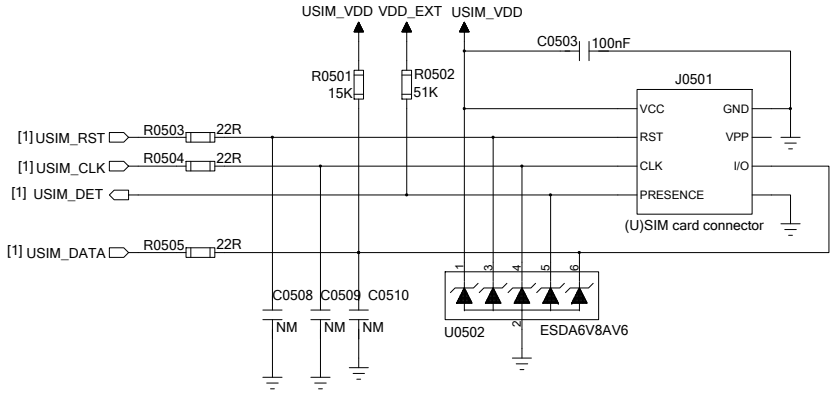
UART Translation - MOSFET Solution



Notes:

1. It is recommended to use an IC conversion chip for UART translation.
   Transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps.
2. Voltage supplied to VCCA should not exceed that of VCCB. For more information about TXS0108E, please refer to the datasheet from Texas Instruments.
3. If a high baud rate is enabled, it is highly recommended to install 1nF capacitors (C0504/C0505/C0506/C0507) on transistor circiuts.
4. The transistor circuit of DTR interface is similar to that of RTS, and the transistor circuits of RI and DCD interfaces are similar to that of CTS.

(U)SIM Interface



Notes:

1. EG12/EG18 module provides two (U)SIM interfaces. The two interfaces have the same design requirements.
2. The decoupling capacitor of USIM_VDD should be less than 1uF and must be placed cloesd to (U)SIM card connector.
3. EG12/EG18 module provides an input pin (USIM_DET) to detect the (U)SIM card. USIM_DET supports both low level and high level detections. For more details, please refer to the hardware design document for corresponding module.
4. R0503~R0505 are applied to suppress the EMI spurious transmission and enhance the ESD protection.
5. Please add an ESD component near the (U)SIM card connector. The TVS diode with junction capacitance less than 50pF must be placed as close as possible to the (U)SIM card connector.
6. R0501 can improve anti-jamming capability of the (U)SIM circuit and it should be placed close to the (U)SIM card connector.
7. The bypass capacitors C0508~C0510 are not mounted by default.

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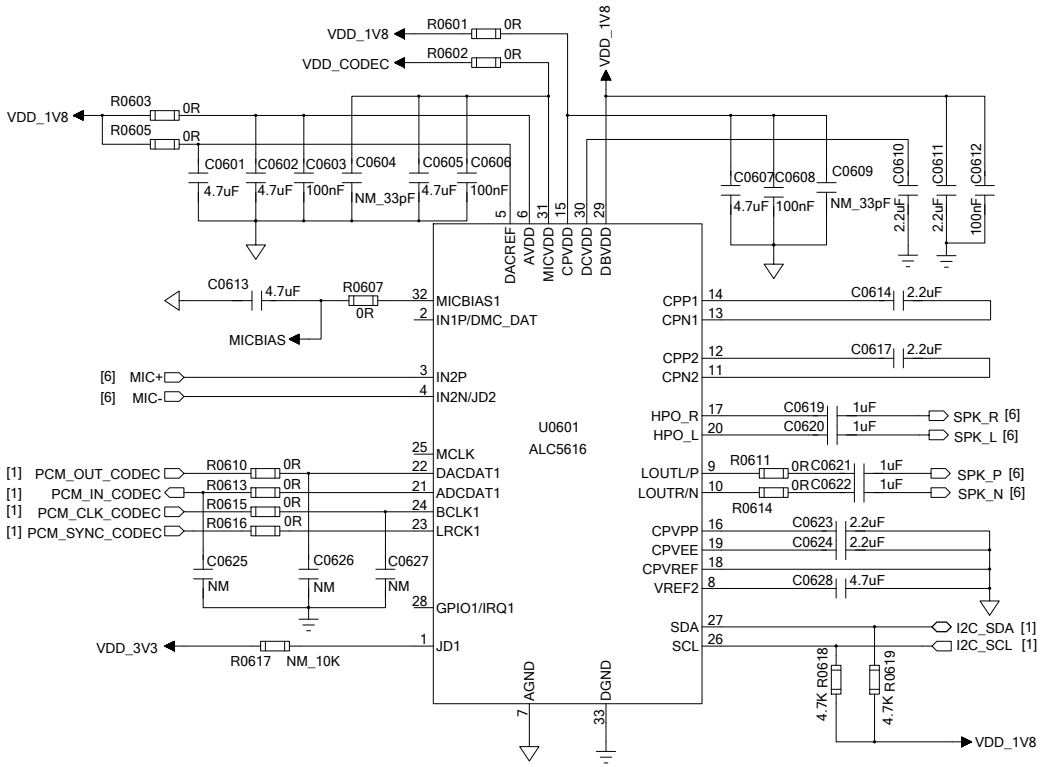
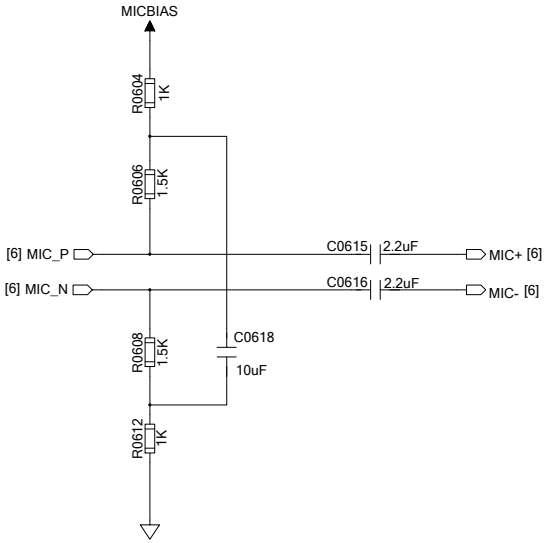
Audio Design

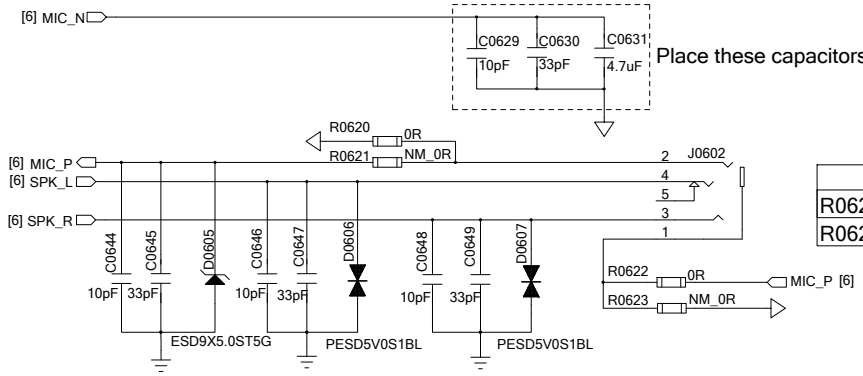




Note:

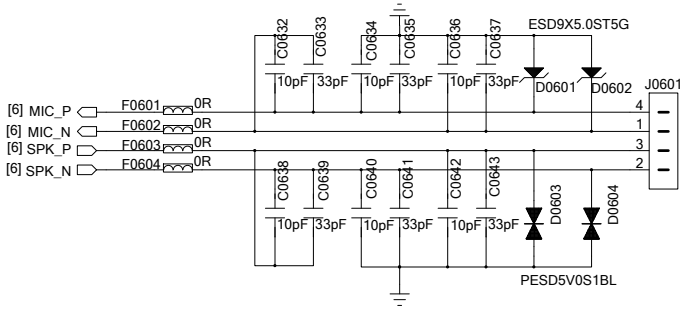
To ensure proper functioning of audio, please follow ALC5616 power-on/off sequence.
Power-on Sequence: VDD_1V8 → VDD_3V3
Power-off Sequence: VDD_3V3 → VDD_1V8
For more details, please refer to ALC5616 datasheet.

Audio - Earphone Application



	CTIA	OMTP
R0621/R0623	NM	M
R0620/R0622	M	NM

Audio - Handset Application



Notes:

1. The analog output only drives earphone and headset. For devices which need larger power loads, such as speakers, an audio power amplifier needs to be added in the design.
2. The maximum capacitive load for speaker is 330pF and the maximum capacitive load for microphone is 250pF.

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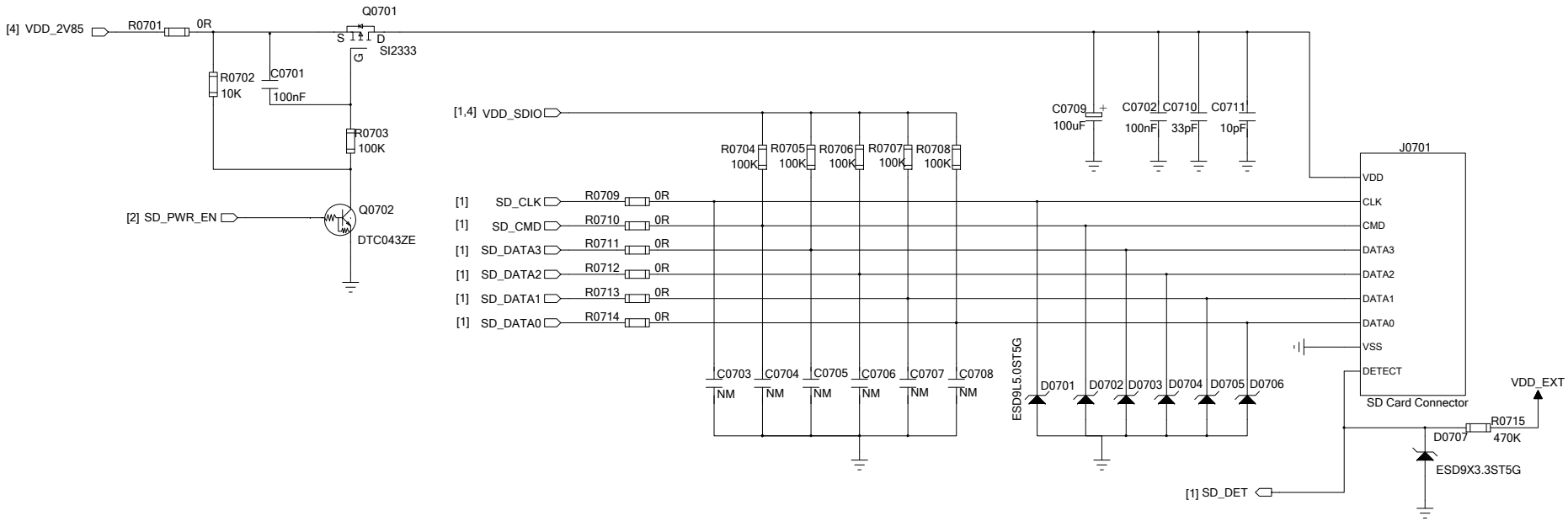
SD Card Design



Notes:

1. VDD_SDIO, with a maximum output current of 50mA, can only be used to supply power for SDIO pull-up resistors.
2. The voltage range of SD card power supply is 2.7~3.6V and a sufficient current up to 0.8A should be provided.
3. To avoid jitter of bus, resistors R0704~R0708 are needed to pull up the SDIO to VDD_SDIO. The value of these resistors is between 10kΩ~100kΩ and the recommended value is 100kΩ.
4. In order to improve signal quality, it is recommended to add 0Ω resistors R0709~R0714 in series between the module and the SD card connector.
   The bypass capacitors C0703~C0708 are not mounted by default. All resistors and bypass capacitors should be placed close to the module.
5. It is recommended to add ESD components near the SD card connector. The parasitic capacitance of ESD components should be smaller than 15pF.
6. Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noisy signals such as clock signals and DC-DC signals.
7. Route SDIO signal traces with 50Ω impedance. It is important to route the SDIO signal traces with total grounding.
8. Make sure the adjacent trace spacing is two times of the trace width and the bus capacitance is less than 40pF.
9. It is recommended to keep the trace length difference between CLK and DATA/CMD less than 1mm and the total exterior trace length should be less than 14mm.
10. DETECT is an active low pin of SD card connector, and it must be connected to the module when an SD card is used.

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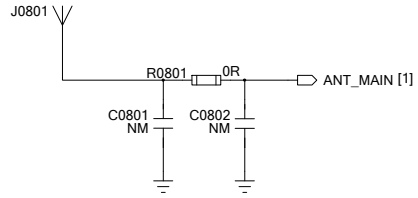
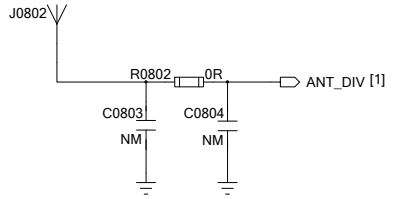
RF and GNSS Design

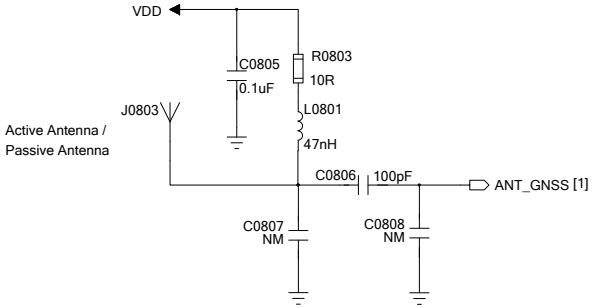
Main Antenna Interface



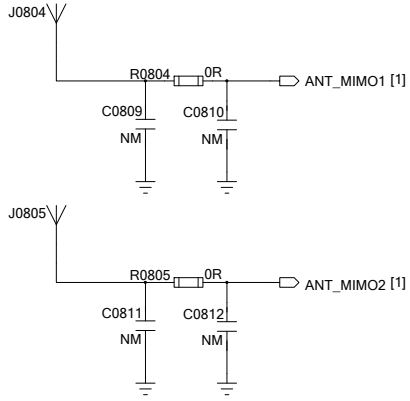
Diversity Antenna Interface



GNSS Antenna Interface



MIMO Antenna Interfaces



Notes:

1. A Pi type circuit is recommended to be used for main antenna and diversity receiving antenna interfaces to facilitate future debugging.
2. The diversity reception function is ON by default.
3. An external LDO can be used in an active antenna circuit to supply power.
4. If a passive antenna is used in the antenna circuit design, then R0803 and L0801 are not needed.
5. ESD protection devices should be added to the GNSS antenna interface, and their parasitic capacitance should be less than 0.05pF.
6. The impedance of the RF signal lines should remain at 50Ω when routing.

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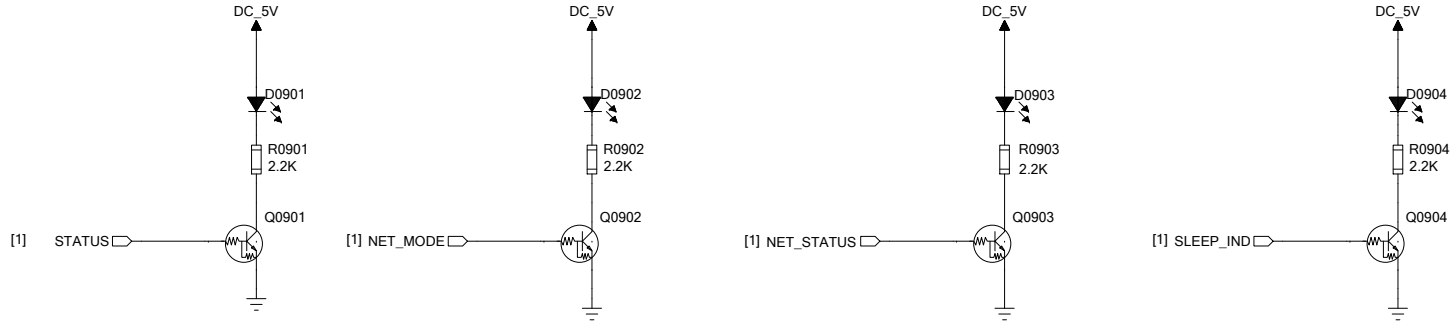
Indicators and Test Points

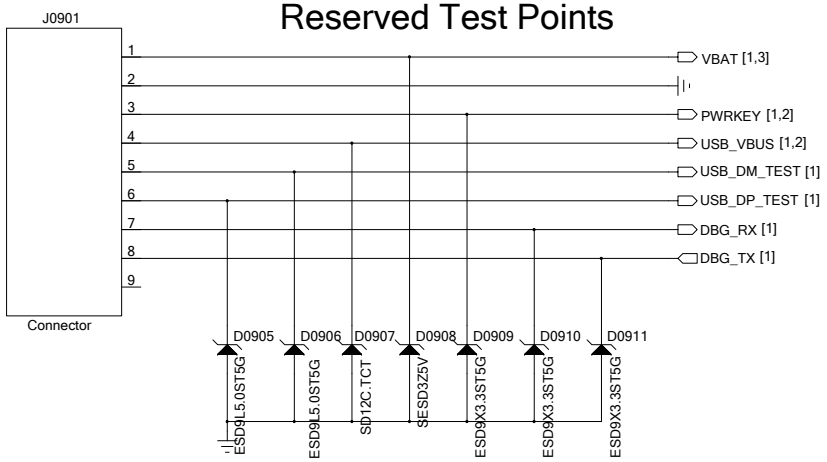
Indicators



Notes:

1. The STATUS is an output pin, and its drive current is less than 1mA.
2. For more details about NET_MODE and NET_STATUS, please refer to the hardware design document for corresponding module.
3. If the current consumption is required to be as low as possible when the device is in sleep, replace the power supply of indicators with a controllable one. And turn off the power when the module enters sleep mode.

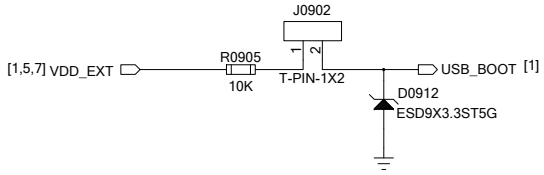
Reserved Test Points



Notes:

1. Both USB and debug UART interfaces are reserved for firmware debugging.
2. USB interface can also be used to upgrade firmware.
3. Keep USB test points as close to USB pins as possible.
   Please pay attention that junction capacitance of ESD components on USB data lines might affect the signal. Thus, the capacitance should be less than 2pF.
4. Debug UART interface supports 1.8V power domain.
   A level translator should be used if the power domain of customers' applications is 3.3V.

Emergency Download Mode



Note:

Developers can pull up USB_BOOT to VDD_EXT before powering on the module, thus the module will enter into emergency download mode when powered on.

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